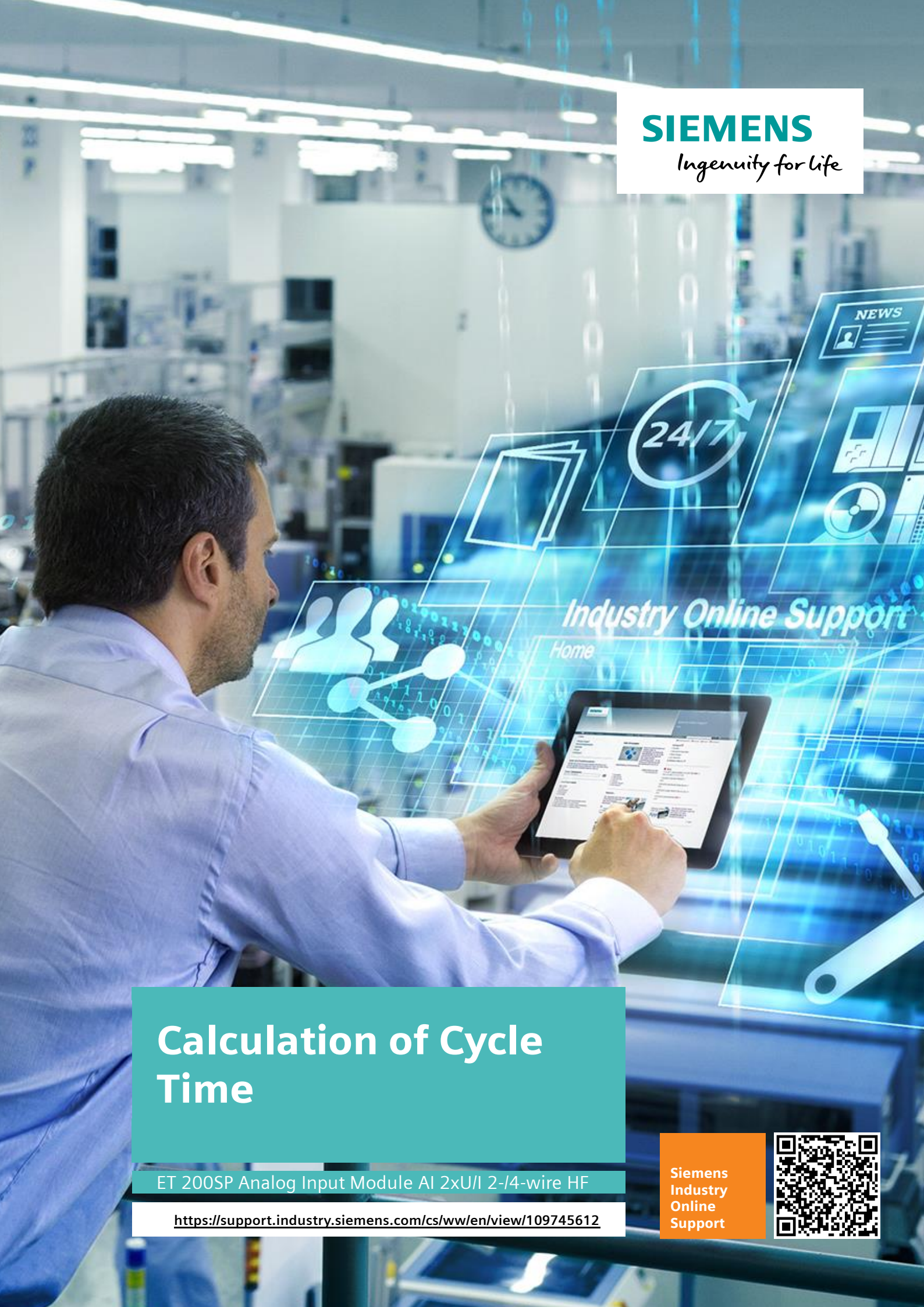

Calculation of Cycle Time

ET 200SP Analog Input Module AI 2xU/I 2-/4-wire HF

https://support.industry.siemens.com/cs/ww/en/view/109745612

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Table of content

1 Introduction

The analog module AI 2xU/I 2-/4-wire HF of the ET 200SP (article number 6ES7134-6HB00-0CA1) is a channel-isolated module that starts conversion for all active channels simultaneously. The conversion time depends on the integration time and therefore on the interference frequency suppression set for the channel. Thus the channel with the longest integration time defines the cycle time of the module, in other words the time interval in which the module supplies new values. In addition, this module synchronizes itself with the backplane (or back wall) bus cycle time of the header module (Interface Module or CPU).

This documentation will explain the basic terms and take you through the calculation based on examples. Figure 2-1 and Table 2-1 show the times specified in the module's data sheet which are needed to calculate the conversion time of a channel and the cycle time of the module.

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2 Conversion Time of a Channel

The conversion time of an individual channel consists of

- The basic conversion time (depending on the parameterized interference suppression) and
- A constant time for measured-value processing (independent of any parameterization).

Figure 2-1 shows the composition of the conversion time of a channel.

Figure 2-1

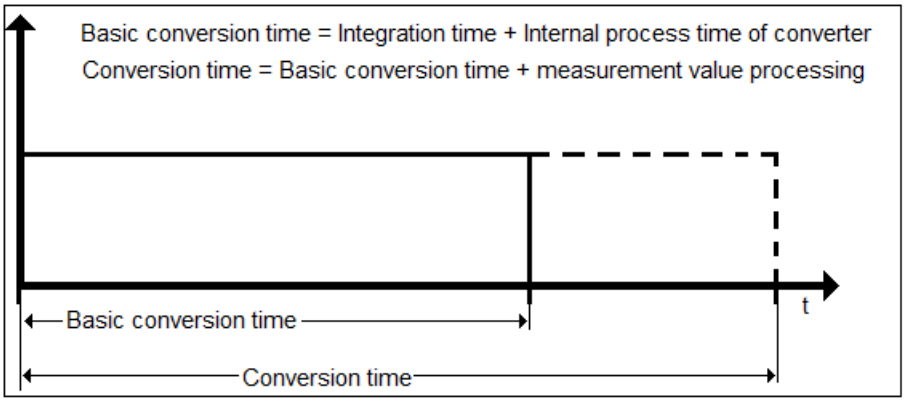

Table 2-1 shows an excerpt from the technical data of the analog module AI 2xU/I 2-/4-wire HF.

Table 2-1

Analog value composition of the inputs	
Measuring principle	Sigma Delta
Integration and conversion time	**Resolution per channel**
Resolution with overrange (bit including sign), max.	16 bits
Parameterizable integration time	Yes
Integration time (ms)	67.5/22.5/18.75/10/5/2.5/1.25/0.625 ms
Basic conversion time including integration time (ms)	68.03/22.83/19.03/10.28/5.23/2.68/1.43/0.73 ms
Interference suppression for interference frequency f1 in Hz	16.6/50/60/300/600/1200/2400/4800
Conversion time (per channel)	68.2/23/19.2/10.45/5.40/2.85/1.6/0.9 ms
Basic execution time of the module (all channel enabled)	1 ms

The technical data of the analog module AI 2xU/I 2-/4-wire HF is available at this link:
https://support.industry.siemens.com/cs/ww/en/pv/6ES7134-6HB00-0CA1

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3 Cycle Time of the Module

The cycle time of the module is synchronized with the backplane bus cycle. You have to calculate the conversion time of the channel with the longest integration time to define the cycle time of the module.
If the conversion time is less than the backplane cycle time, the cycle time of the module is that of the backplane bus cycle.

If the conversion time is greater than the backplane cycle time, this is reduced in the module by a multiple of 2^n (n = 0, 1, 2, …) until the conversion time can be mapped in it with respect to time. The reduced backplane bus cycle time is then that of the cycle time of the module for both channels.

The next chapter gives examples illustrating this.

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4 Sample Calculations of Conversion Time and Cycle Time

4.1 Channels are Parameterized the Same and the Conversion Time is Less Than the Backplane Bus Cycle

Backplane bus cycle:

- **1 ms**

Channel parameters:

In this example the channels have the same parameters.

- Channel 0 with interference suppression 4.8 kHz (0.625 ms)
- Channel 1 with interference suppression 4.8 kHz (0.625 ms)

Calculation of the module cycle time:

The conversion of both channels is started simultaneously. Since both channels have the same integration time this defines the cycle time of the module. The following times are given in the Technical Data:

Table 4-1

Analog value composition of the inputs	
Measuring principle	Sigma Delta
Integration and conversion time	**Resolution per channel**
Resolution with overrange (bit including sign), max.	16 bits
Parameterizable integration time	Yes
Integration time (ms)	67.5/22.5/18.75/10/5/2.5/1.25/**0.625 ms**
Basic conversion time including integration time (ms)	68.03/22.83/19.03/10.28/5.23/2.68/1.43/**0.73 ms**
Interference suppression for interference frequency f1 in Hz	16.6/50/60/300/600/1200/2400/**4800**
Conversion time (per channel)	68.2/23/19.2/10.45/5.40/2.85/1.6/**0.9 ms**
Basic execution time of the module (all channel enabled)	1 ms

Table 4-2

Description	Times
Integration time with interference frequency suppression of 4.8 kHz	0.625 ms
Basic conversion time incl. integration time	0.730 ms
Conversion time (basic conversion time + 0.170 ms)	0.900 ms

This results in a conversion time of 0.900 ms. Since this conversion time is less than the backplane bus cycle time of 1 ms, reduction is not necessary.

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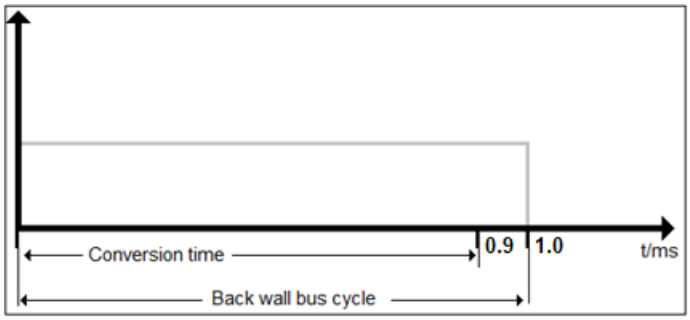
A conversion time of 0.900 ms therefore results in a module cycle time of 1 ms.

Figure 4-1



4.2 Channels are Parameterized Differently and the Conversion Time is Greater Than the Backplane Bus Cycle

Backplane bus cycle:

- **1 ms**

Channel parameters:

In this example the channels are parameterized differently.

- Channel 0 with interference suppression 50 Hz (22.5 ms)
- Channel 1 with interference suppression 4.8 kHz (0.625 ms)

Calculation of the module cycle time:

The conversion of both channels is started simultaneously. Since channel 0 has a longer integration time this defines the cycle time of the module. The following times are given in the Technical Data:

Table 4-3

Analog value composition of the inputs	
Measuring principle	Sigma Delta
Integration and conversion time	**Resolution per channel**
Resolution with overrange (bit including sign), max.	16 bits
Parameterizable integration time	Yes
Integration time (ms)	67.5/**22.5**/18.75/10/5/2.5/1.25/**0.625 ms**
Basic conversion time including integration time (ms)	68.03/**22.83**/19.03/10.28/5.23/2.68/1.43/**0.73 ms**
Interference suppression for interference frequency f1 in Hz	16.6/**50**/60/300/600/1200/2400/**4800**
Conversion time (per channel)	68.2/**23**/19.2/10.45/5.40/2.85/1.6/**0.9 ms**

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Table 4-4

Description	Times
Integration time with interference frequency suppression of 50 Hz	22.500 ms
Basic conversion time incl. integration time	22.830 ms
Conversion time (basic conversion time + 0.170 ms)	23.000 ms

This results in a conversion time of 23.000 ms. This conversion time now has to be synchronized with the backplane bus cycle in order to be able to define the module cycle time.

In the example it is assumed that there is a backplane bus cycle of 1 ms. The synchronization can only be done to a multiple of 2^n (n = 0, 1, 2, …). The following relevant reduction factors are therefore available for the example:

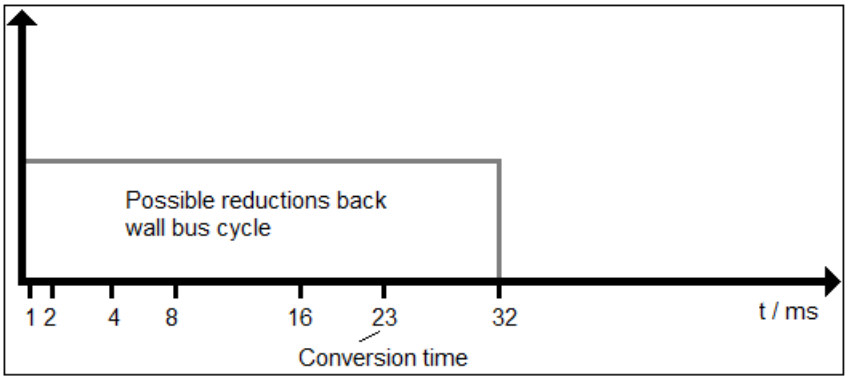
- 1 / 2 / 4 / 8 / 16 / 32

Multiplied by the backplane bus cycle time of 1 ms this gives:

- 1 / 2 / 4 / 8 / 16 / 32 ms

In this way a conversion time of 23.000 ms gives a module cycle time of 32 ms.

Figure 4-2



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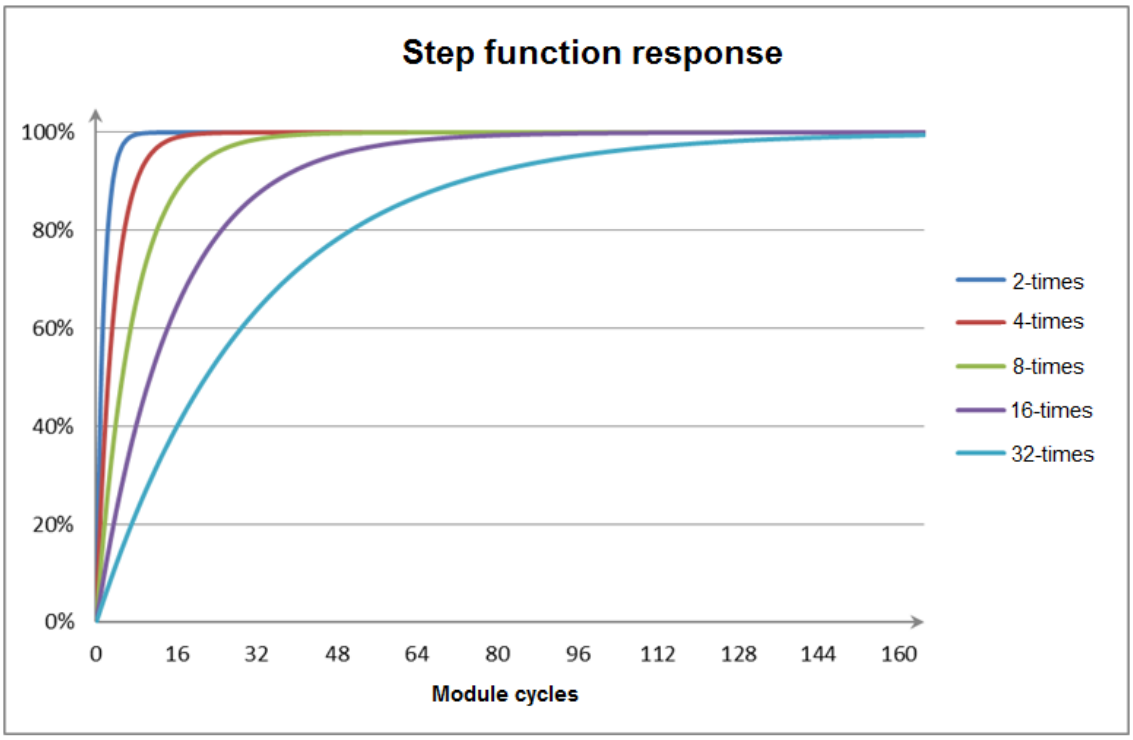
5 Influence of the Cycle Time on Smoothing

The additional digital filtering of the analog value that can be set via the "Smoothing" parameter takes the module cycle time as a time base. As described in the previous chapters this is determined mainly by the "Interference frequency suppression" parameter. The exponential smoothing procedure used gives the following duration time for a step-function response of the input signal to about 99% of the end value:

- 5 x smoothing factor x module cycle time.

The different step-function response times with reference to the module cycles are shown in the following Figure 5-1.

Figure 5-1



With a smoothing factor of 32 the calculation in the example in section 4.2 produces a step-function response time of 5 x 32 x 32 ms = 5120 ms.

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