Function Block for Monitoring 24V Load Circuits

SITOP PSE200U, STEP 7 (TIA Portal) V14

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1 Introduction

1.1 Overview

The SITOP PSE200U electronic selectivity module is designed to be connected to a controlled 24V DC power supply with up to 40 A output current. The selectivity module allows the 24 V DC output voltage generated by a controlled power supply to be split between four load circuits. For each output, the rated current can be set individually with a potentiometer in the range from 0.5A to 3A or from 3A to 10A, respectively, depending on the type. If the rated current exceeds these values, the output will be disabled after a certain period of time and can be re-enabled using buttons on the selectivity module or via remote reset after a certain waiting time has elapsed.

1.2 Mode of operation

The status output (S) of the selectivity module supplies a signal that serially codes the state of the 4 load circuits.

The signal of status output (S) of the S7 CPU is read and evaluated via a digital input. This allows you to monitor the status of outputs 1 to 4 via the application program of the S7-CPU.

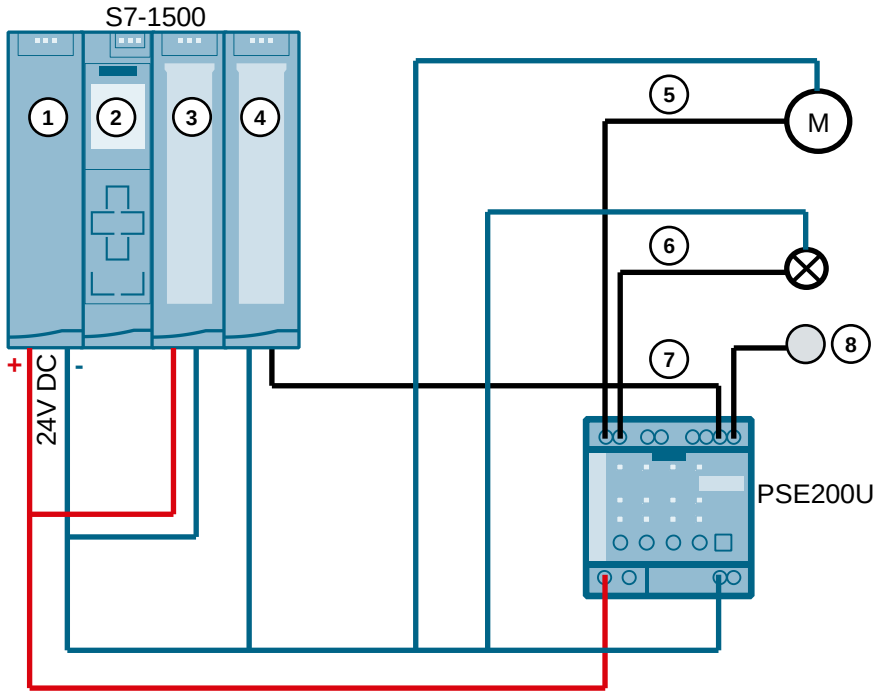
The S7-CPU detects, whether the consumer connected to output 1, e.g., a motor, has produced an overload.

The S7-CPU detects, whether the consumer connected to output 2, e.g., a light, has produced a short-circuit.

1.2.1 Application with S7-1500

The following figure shows the monitoring of 24V load circuits by the SITOP PSE200U selectivity module and S7-1500 CPU.

Figure 1-1

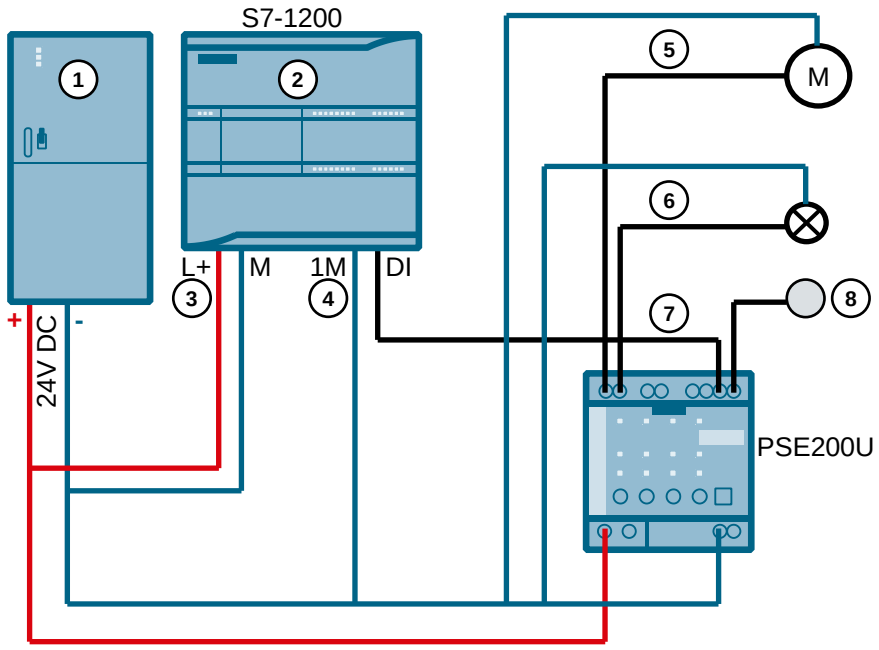


1 Power supply
2 CPU with FB “LSitopPseDiag”
3 Digital input module (DI)
4 Digital output module (DO)
5 Output 1
6 Output 2
7 Status output
8 Remote reset

1.2.2 Application with S7-1200

The following figure shows the monitoring of 24V load circuits by the SITOP PSE200U selectivity module and S7-1200 CPU.

Figure 1-2

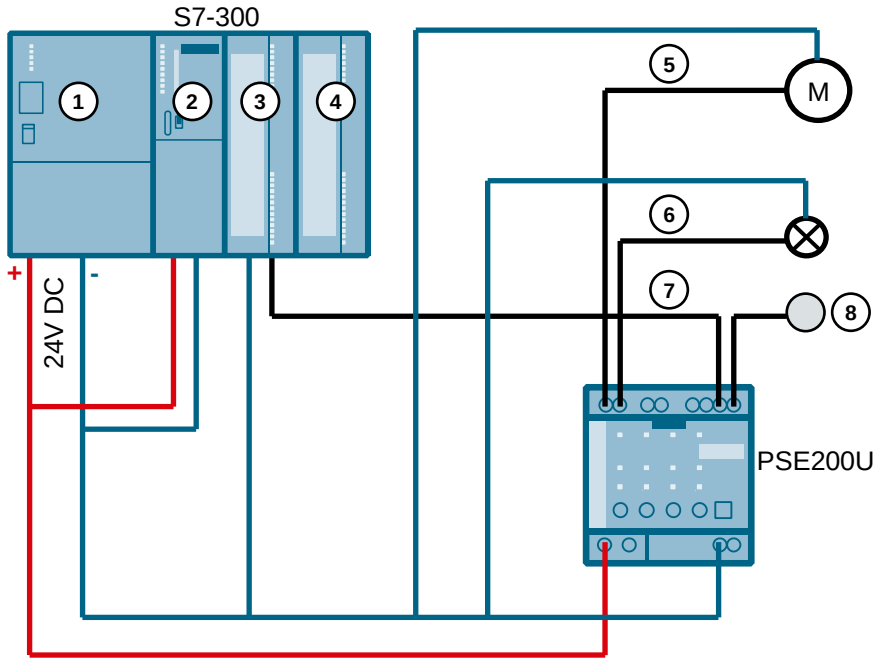


1 Power supply
2 CPU with FB “LSitop_PseDiag”
3 X10 (24V DC)
4 X11 (24V DC INPUTS)
5 Output 1
6 Output 2
7 Status output
8 Remote reset

1.2.3 Application with S7-300/S7-400

The following figure shows the monitoring of 24V load circuits by the selectivity module SITOP PSE200U and S7-300/S7-400 CPU.

Figure 1-3

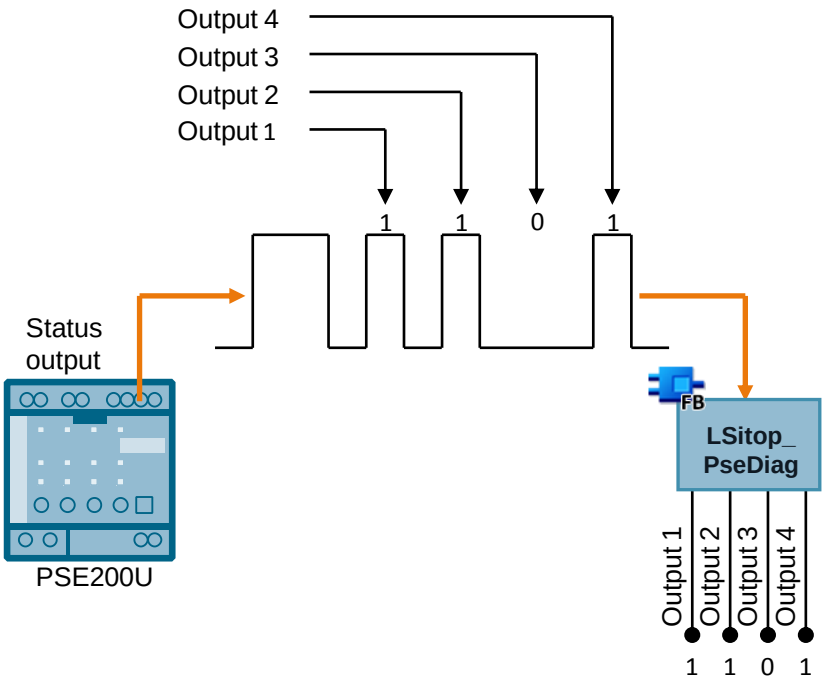


1 Power supply
2 CPU with FB “Lsitop_PseDiag”
3 Digital input module (DI)
4 Digital output module (DO)
5 Output 1
6 Output 2
7 Status output
8 Remote reset

1.2.4 Workflow

The LSitop library supplies the "LSitop_PseDiag" function block each for S7-1500 CPUs, S7-1200 CPUs and S7-300/S7-400 CPUs. Call the "LSitop_PseDiag" function block in the user program of the S7-CPU in order to evaluate the signal of the status output (S). The "LSitop_PseDiag" function block reads the signal of the status output (S) via an input and displays the state of the four outputs of the selectivity module on its output.

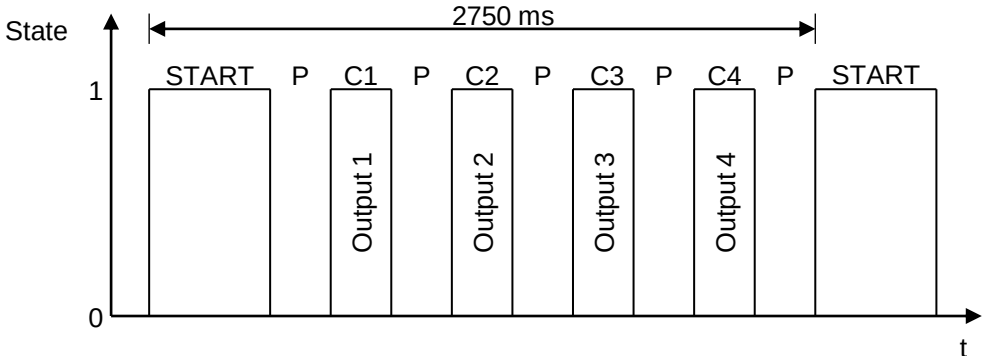
Figure 1-4



1.2.5 Signal trend of the status output (S)

Figure 1-5 shows the signal trend of the status output (S). A signal frame consists of one start bit and four channel bits that are each separated by a pause bit. The start bit is always "1" and the pause bits are always "0". The channel bits signal the status of the outputs 1 to 4.

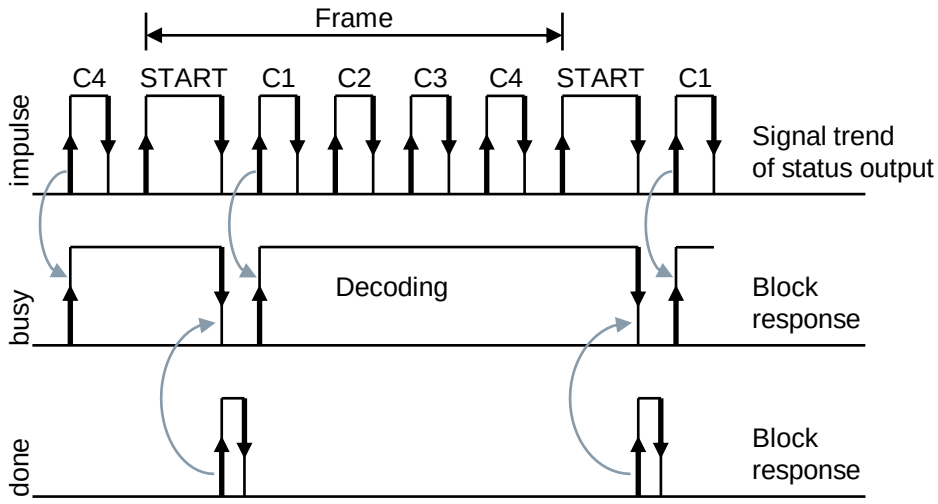
Figure 1-5



1.2.6 Functional sequences of the "LSitop_PseDiag" function block

Figure 1-6 shows the graphic representation of the functional sequence of the "LSitop_PseDiag" function block.

Figure 1-6



1.2.7 Internally used instructions for S7-1500 CPUs and S7-300/S7-400 CPUs

For the S7-1500 CPUs and S7-300/S7-400 CPUs the following instructions are used internally in the "LSitop_PseDiag" function block:

- TIME_TCK: The TIME_TCK instruction reads the system time from the CPU. The system time is a time counter that counts from 0 to max. 2147483647ms. If an overflow occurs, counting is started again at "0". The time grid and the precision of the system time is 1ms. The system time is used in the "LSitop_PseDiag" function block to calculate the cycle time as well as the length of the pulses and pauses.
  The TIME_TCK instruction can be found in the task card "Instructions" > tab "Extended Instructions > "Date and time-of-day" > "Clock functions".
- TON: This instruction generates a switch-on delay. The switch-on delay is used for the generation of the error messages in the "LSitop_PseDiag" function block.
  You can access the TON instruction via the task card "Instructions > tab "Basic instructions > Timer operations".

Comparing time values

To calculate the cycle time and the length of the pulses and pauses, the read system time must be higher than the time read and saved in the last cycle. This means that relational expressions are used in the function block to compare for higher values of the contents of two variables of TIME data type.

Calculating cycle time

To calculate the cycle time, the system time read in every cycle is saved and subtracted from the newly read system in the next cycle. The cycle time may be max. 100 ms so that each pulse can be detected in the signal trend of the status output (S). If the cycle time exceeds 100 ms, the "LSitop_PseDiag" function block will output an error with the value 16#8001 on the "status" output.

Calculating the length of a pulse

In order to calculate the length of a pulse, the system time is read and saved when a positive edge is detected on the "impulse" input. When a negative edge is subsequently detected, the system time is read and saved again. The system time saved for a positive edge is subtracted from the saved system time for a negative edge.

Calculating the length of a pause

In order to calculate the length of a pause, the system time is read and saved when a negative edge is detected on the "impulse" input. When a positive edge is subsequently detected, the system time is read and saved again. The system time saved for a negative edge is subtracted from the saved system time for a positive edge.

1.2.8 Internally used instructions for S7-1200 CPUs

For the S7-1200 CPUs the following instructions are used internally in the "LSitop_PseDiag" function block:

- RD_SYS_T: The RD_SYS_T instruction reads the current date and the current time (module time) from the CPU clock. The time is used in the "LSitop_PseDiag" function block to calculate the cycle time as well as the length of the pulses and pauses.
  You can access the RD_SYS_T instruction in the task card "Instructions" > tab "Extended Instructions > Date and time-of-day".
- TON: This instruction generates a switch-on delay. The switch-on delay is used for the generation of the error messages in the "LSitop_PseDiag" function block.
  You can access the TON instruction via the task card "Instructions > tab "Basic instructions > Timer operations".
- T_DIFF: This instruction is used to calculate the difference between two instants of time by subtracting two instants of times of the DT format.
  You can access the T_DIFF instruction via the task card "Instructions" > tab "Extended Instructions > Date and time-of-day".

Comparing time values

To calculate the cycle time and the length of the pulses and pauses, the read time must be higher than the time read and saved in the last cycle. This means that relational expressions are used in the function block to compare for higher values of the contents of two variables of "DTL" data type.

Calculating cycle time

To calculate the cycle time, the exported time of any cycle is saved and subtracted from the new time read in the next cycle. The cycle time must be max. 100 ms so that each pulse can be detected in the signal trend of the status output (S). If the cycle time exceeds 100 ms, the "LSitop_PseDiag" function block will output an error with the value 16#8001 on the "status" output.

Calculating the length of a pulse

In order to calculate the length of a pulse, the time is read and saved when a positive edge is detected on the "impulse" input. When a negative edge is subsequently detected the time is read and saved again. The time saved for a positive edge is subtracted from the time saved for a negative edge.

Calculating the length of a pause

In order to calculate the length of a pause, the time is read and saved when a negative edge is detected on the "impulse" input. When a positive edge is subsequently detected, the time is read and saved again. The time saved for a negative edge is subtracted from the time saved for a positive edge.

Note Since the time is used in the S7-1200 for calculating the cycle time and the length of the pulses and pause, the "channelState" output must not be evaluated when the time is set by clock synchronization (see chapter 3.1.2).

1.2.9 Mode of operation of the selectivity module

A multi-color LED display front panel of the device indicates the mode of the respective outputs.

Table 1-1 shows which mode has the effect that outputs 1 to 4 to switch to state 0 or 1, respectively, during the signal trend of the status output (S).

Table 1-1

LED displays	Mode	Status output 1 to 4
off	All LED displays: • Supply voltage missing • Start-up of the device: Once the start-up of the device is accomplished, the outputs will be switched on whilst considering the set connect delay.	During startup or when the supply voltage is missing there will be no signaling on the status output. The status is continuously 0.
	LED display of individual output: • Output defective (internal fuse has tripped)	0
Lights up green	Normal operation, output connected	1
Flashing green	Overload on output: Output current 101 to 150% of response threshold (admissible for 5s)	1
Lights up red	Output switched off due to overload	0
Flashing red	Output ready for reset of automatic switch-off by clicking the button on the selectivity module or the remote reset (effective for all automatically switched off outputs)	0
Flashing orange	Output manually switched off by clicking a button on the selectivity module: The state is saved when the device is switched off and can only be reset by pressing the button again.	0
Red chaser light	Excessive temperature of device: Once the excessive temperature has cooled down, the outputs can be switched on again.	0

1.3 Components used

This application example was created with the following hardware and software components:

Table 1-2

Component	Number	Article number	Alternative
SITOP			
SITOP PSE200U 3A with single-channel signaling (selectivity module)	1	6EP1961-2BA31	• SITOP PSE200U 10A, article number: 6EP961-2BA41 • SITOP PSE200U 3A NEC Class 2, article number: 6EP961-2BA51 6EP961-2BA61
S7-1500			
S7-CPU	1	6ES7513-1AL00-0AB0	any S7-1500 CPU and ET 200SP CPU
Digital input module DI 32x24VDC HF	1	6ES7521-1BL00-0AB0	other digital input modules or digital inputs of a distributed I/O
Digital output module DQ 16x24VDC/0.5A ST	1	6ES7522-1BH00-0AB0	other digital output modules or digital outputs of a distributed I/O
S7-1200			
S7-CPU	1	6ES7214-1AG40-0AB0	any S7-1200 CPU
S7-300/S7-400			
S7-CPU	1	6ES7315-2EH14-0AB0	• Any S7-300/S7-400 CPU • IM 151-8(F) PN/DP CPU • IM 154-8(F/FX) PN/DP CPU
DI 8/DO 8x24VDC/0.5A	1	6ES7323-1BH01-0AA0	other digital input modules and digital output modules or digital inputs and outputs of a distributed I/O
Engineering software			
STEP 7 (TIA Portal) V14 Upd2	1	6ES7822-1AA04-0YA5	You require STEP 7 Professional (TIA Portal) V14 SP Upd2 or higher for the configuration of the S7 CPU.

2 Engineering

2.1 Interface description

The "LSitop_PseDiag" function blocks reads the status output (S) via the "impulse" input of the selectivity module in order to evaluate the signal trend of the status output (S) and to display the state of outputs 1 to 4 on the "channelState" output.

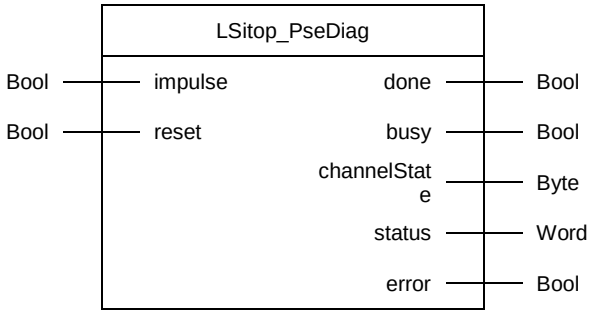
Figure 2-1 shows the call of the "LSitop_PseDiag" function block in the user program.

Call the "LSitop_PseDiag" function block in the user program of the S7-CPU cyclically in OB1 or in an interrupt OB with max. 100 ms.

The cycle time may be max. 100 ms so that each pulse is detected in the signal trend of the status output (S).

Note If the cycle time exceeds 100 ms, the "LSitop_PseDiag" function block will output an error with the value 16#8001 on the "status" output.

Figure 2-1



The following table shows the parameters of the "LSitop_PseDiag" function block.

Table 2-1

Name	P type	Data type	Comment
impulse	IN	Bool	Input via which the signal of the status output of the selectivity module is read. Figure 1-5 shows the signal trend of the status output (S).
reset	IN	Bool	A reset is tripped on positive edge. All parameters (static variables and outputs of the "LSitop_PseDiag" function block) are reset.
done	OUT	Bool	done = 1: A frame was evaluated completely and without error. The state of outputs 1 to 4 of the selectivity module is displayed on the "channelState" output. The data of the "channelState" output can be accepted. The value done = 1 is set for one cycle. done = 0: Frame evaluation is running or no signal detected on "impulse" input.

Name	P type	Data type	Comment
busy	OUT	Bool	busy = 1: Function block "LSitop_PseDiag" is active busy = 0: If done = 1 a frame was evaluated completely and without error. The state of outputs 1 to 4 of the selectivity module is displayed on the "channelState" output. The data of the "channelState" output can be accepted.
channelState	OUT	Byte	Status of outputs 1 to 4 Bit 0 = 1 if output 1 has status 0 Bit 0 = 0 if output 1 has status 1 Bit 1 = 1 if output 2 has status 0 Bit 1 = 0 if output 2 has status 1 Bit 2 = 1 if output 3 has status 0 Bit 2 = 0 if output 3 has status 1 Bit 3 = 1 if output 4 has status 0 Bit 3 = 0 if output 4 has status 1 Bit 4: not assigned Bit 5: not assigned Bit 6: not assigned Bit 7: not assigned Table 1-1 Gives an overview of the modes and the status of outputs 1 to 4.
status	OUT	Word	Status indication: If error = 1 the error code for one cycle is displayed on the "status" output. If error = 0 the value 16#0000 is displayed at the "status" output.
error	OUT	Bool	• error = 1: An error occurred during the execution of the routine. The value error = 1 is set for one cycle. • error = 0: no error

Note The instance DB of the "LSitop_PseDiag" function block is generated when the "LSitop_PseDiag" function block is called up. For each call of the "LSitop_PseDiag" function block you require an independent instance DB. The "LSitop_PseDiag" function block must not be called up more than once with the same instance DB.

Status indication

Table 2-2

Value on the "status" output	Meaning	Remedy/note
16#8001	100 ms cycle time exceeded	Call the "LSitop_PseDiag" function block with max. 100 ms.
16#8002	No signal change was detected on the "impulse" input for at least 6 s.	• Check whether the status output (S) of the selectivity module is connected to the digital input. • Check whether you specified the correct digital input on the "impulse" input. • Check if the power supply is connected to the selectivity module.

2.2 Integration into the user project

Below, you find the steps necessary for integrating the LSitop library into your STEP 7 project. Once the integration process is complete, you can use the function blocks of the LSitop library.

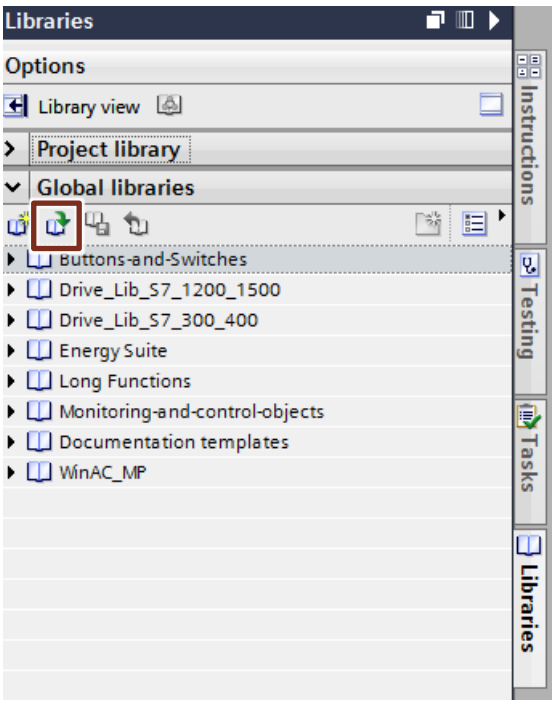
Note In the following section it is assumed that a STEP 7 project has been created.

1. The library is available on the HTML page from which you downloaded this document. Save the "61450284_PSE200U_STEP7_V14_LIB_V23.zip" library on your hard drive.
2. Unzip the library.
3. Once you have unzipped the library, open it in STEP 7 V14.
   Prerequisite
   The "Libraries" task card is displayed.

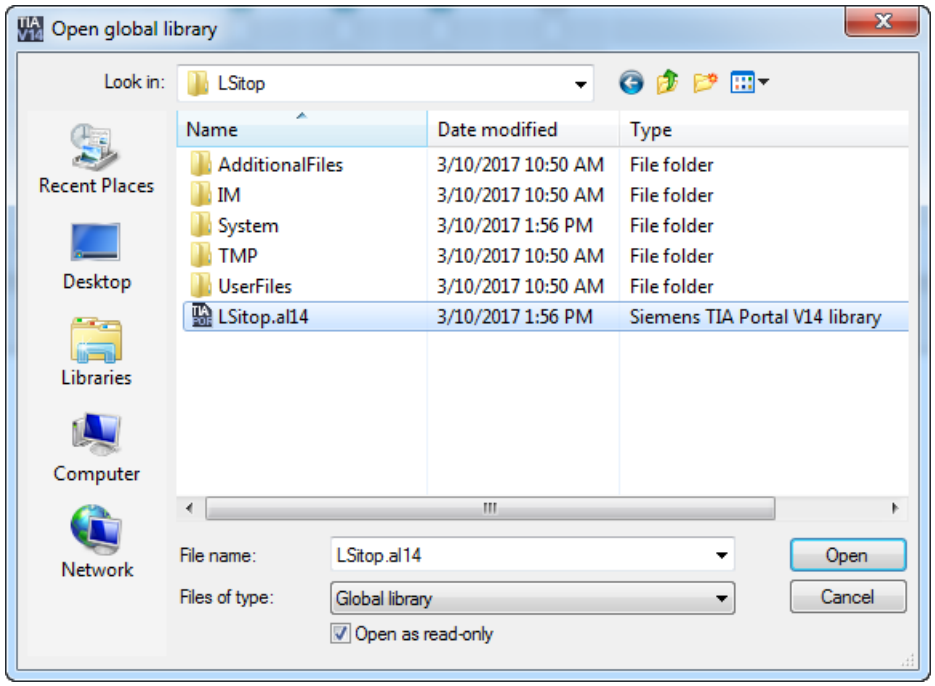
2.2.1 Opening the LSitop library in STEP 7

To open the LSitop library, proceed as follows:

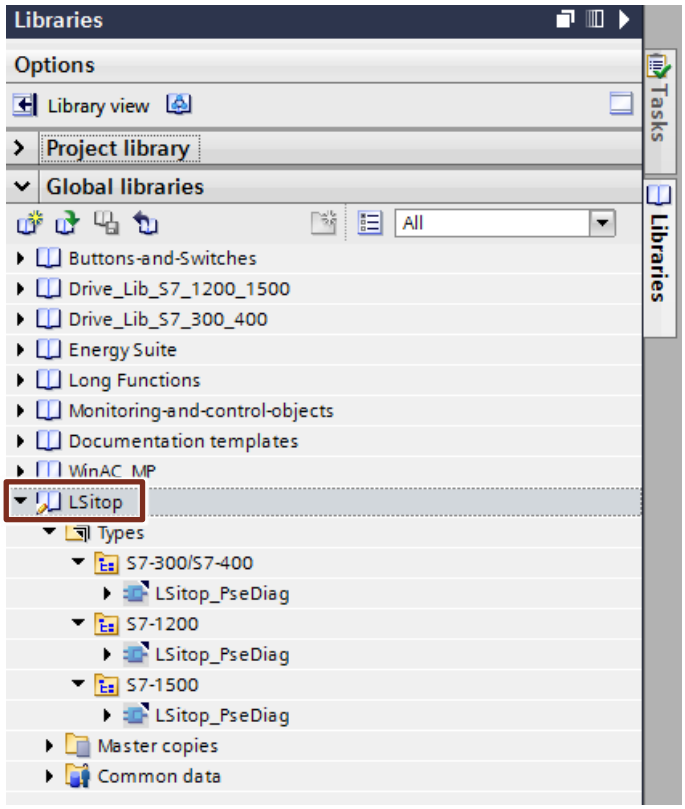
1. Click "Open global library" in the toolbar of the "Global Libraries" tab, or select the "Global libraries" > "Open library" command in the "Options" menu. The "Open global library" dialog box opens.



2. Select the LSitop global library. You can identify the library file by the file name extension ".al14". Click the "Open" button.



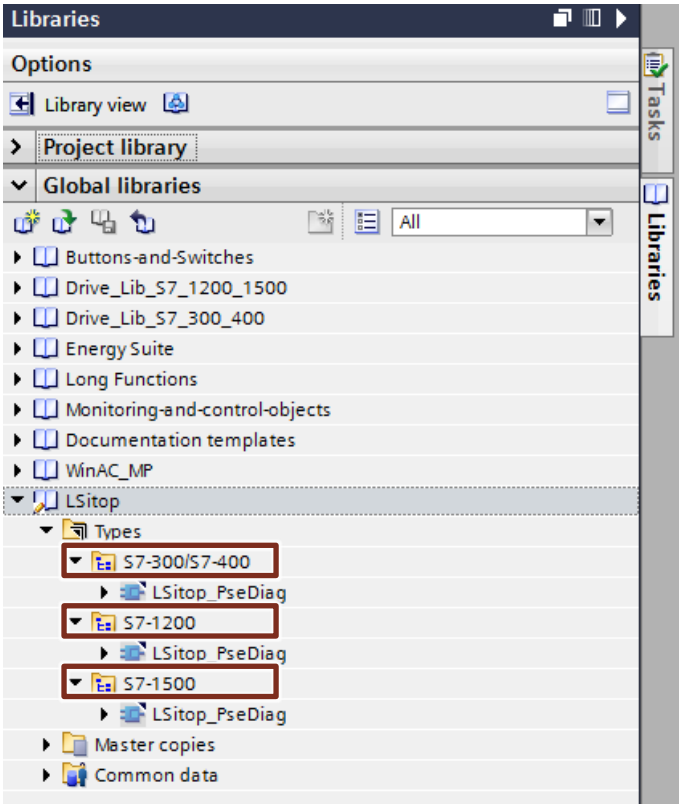
3. The LSitop library is opened and inserted into the "Global libraries" tab.



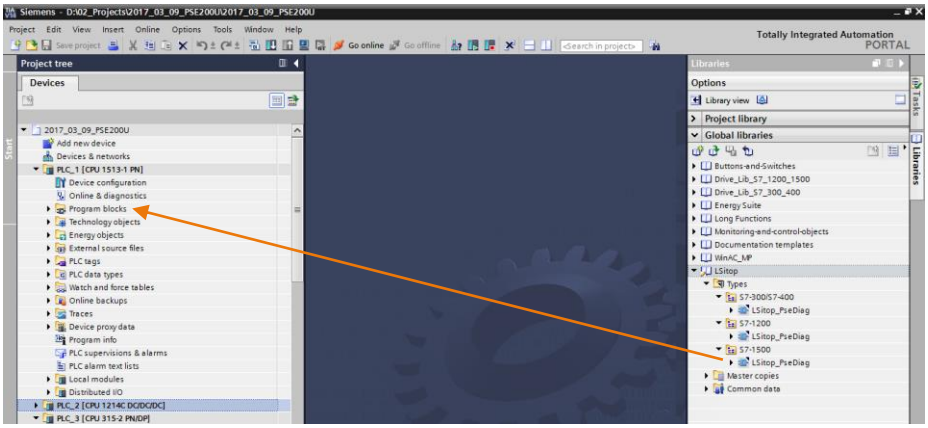
2.2.2 Integrating the library blocks into the STEP 7 project

To integrate the blocks of the LSitop library into your STEP 7 project, proceed as follows:

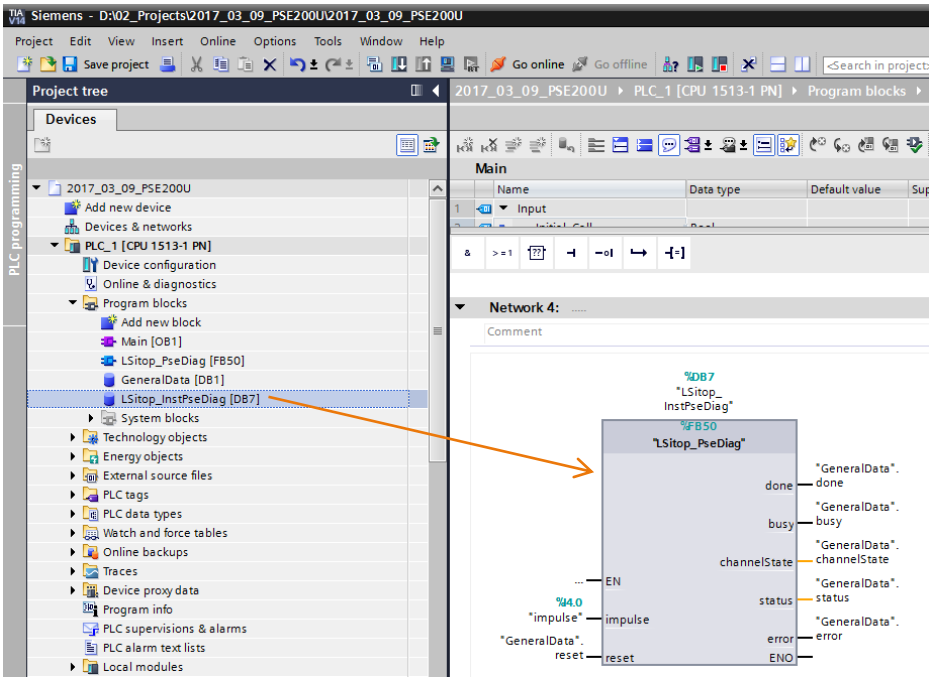
1. Once you have opened the LSitop library, open your STEP 7 project.
2. The "LSitop_PseDiag" function block each for S7-1500 CPUs, S7-1200 CPUs and S7-300/S7-400 CPUs can be found in the "Types" folder of the LSitop library.



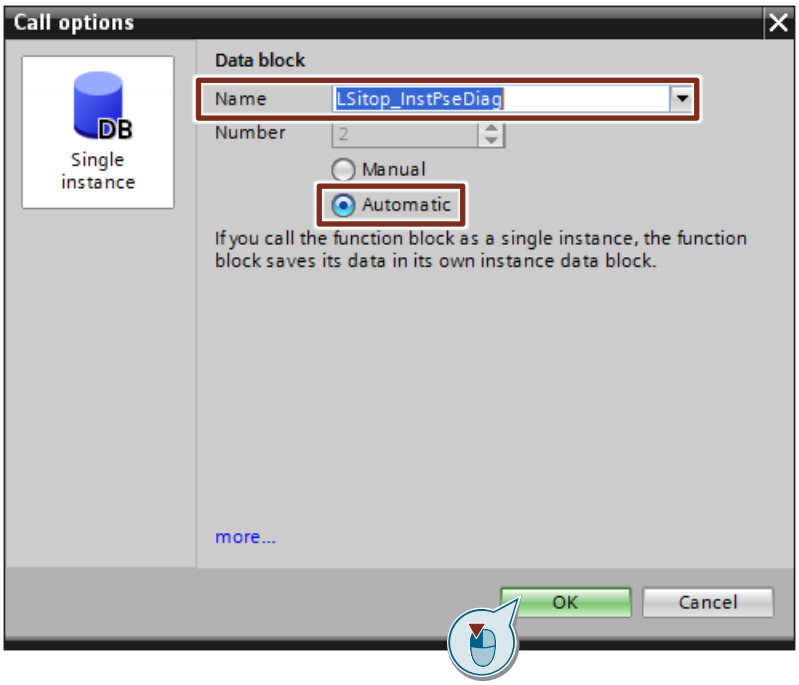
3. Use drag-and-drop to insert the blocks of the LSitop library into the "Program blocks" folder of your device, for example the S7-1500 CPU.



4. Open the OB Main (OB1) in the project tree in the "Program blocks" folder of the CPU. Now use drag-and-drop to move the "LSitop_PseDiag" function block from the project tree to any network of the OB Main (OB1). The "Call options" dialog opens automatically to generate the instance DB of the "LSitop_PseDiag" function block.



5. Make the following settings in the "Call options" dialog.
   - Enter the name of the instance data block.
   - Enable the "Automatic" function to let the STEP 7 (TIA Portal) automatically generate the number of the instance data block.
   - Click "OK" to exit the dialog box.

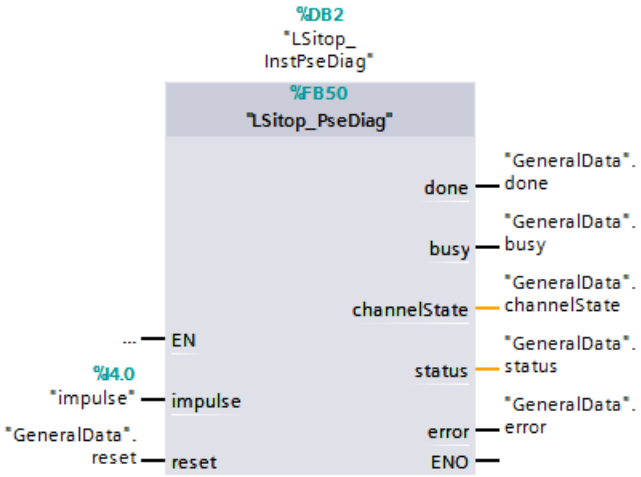


6. If you are using an S7-300/S7-400, open the newly generated new instance data block and disable the "Retain" option for all the variables of the instance DB. On CPU restart, the variables of the instance DB are thus overwritten with the defined initial values.
   For the S7-1500/S7-1200, this setting is made during the interface definition in the " LSitop_PseDiag" function block. Thus, the "Retain" option is automatically disabled when generating the instance DB.

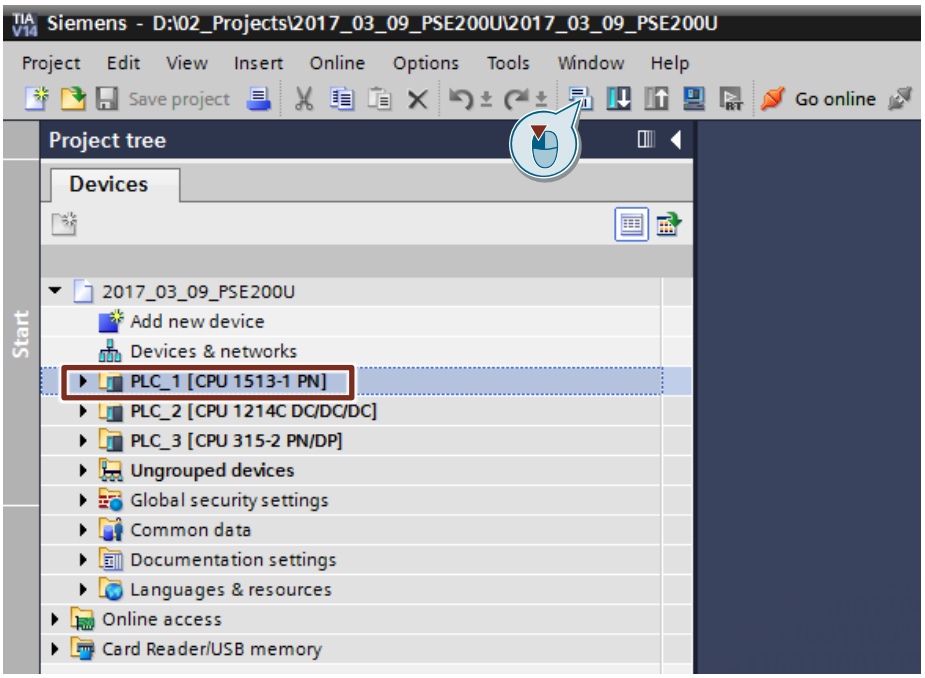
LSitop_InstPseDiag

	Name	Data type	Offset	Start value	Retain
1	Input				
2	impulse	Bool	0.0	false	
3	reset	Bool	0.1	false	
4	Output				
5	done	Bool	2.0	false	
6	busy	Bool	2.1	false	
7	channelState	Byte	3.0	16#0	
8	status	Word	4.0	16#0	
9	error	Bool	6.0	false	
10	InOut				
11	Static				
12	statImpulseOld	Bool	8.0	false	
13	statResetOld	Bool	8.1	false	
14	statTimeSaver	Struct	10.0		
15	statDeltaTimeImpulse	Time	22.0	T#0ms	
16	statDeltaTimePause	Time	26.0	T#0ms	
17	statStartImpulseDetected	Bool	30.0	false	
18	statImpulseDetected	Bool	30.1	false	
19	statChannelState	Byte	31.0	16#0	
20	statTimePauseSave0	Time	32.0	T#0ms	
21	statTimePauseSave1	Time	36.0	T#0ms	
22	statTimePauseSave2	Time	40.0	T#0ms	
23	statTimePauseSave3	Time	44.0	T#0ms	
24	statTimePauseSave4	Time	48.0	T#0ms	
25	statTimeImpulseSave0	Time	52.0	T#0ms	
26	statTimeImpulseSave1	Time	56.0	T#0ms	
27	statTimeImpulseSave2	Time	60.0	T#0ms	
28	statTimeImpulseSave3	Time	64.0	T#0ms	
29	statTimeImpulseSave4	Time	68.0	T#0ms	
30	statFrameImulseDetected	Bool	72.0	false	
31	statNumberOfImpulses	Int	74.0	0	

7. Assign values to all the necessary formal parameters.



8. Save the project.
9. Select the CPU in the project tree and click the "Compile" button in the toolbar.

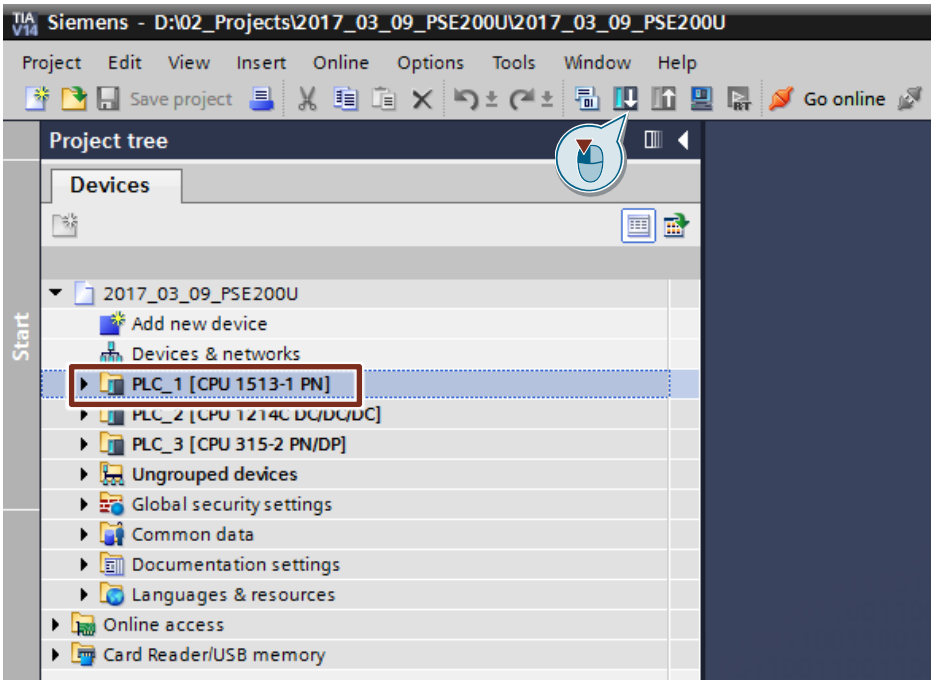


2.2.3 Downloading the library blocks to the S7-CPU

Below, you find the steps necessary to download all blocks of your application program to the S7-CPU.

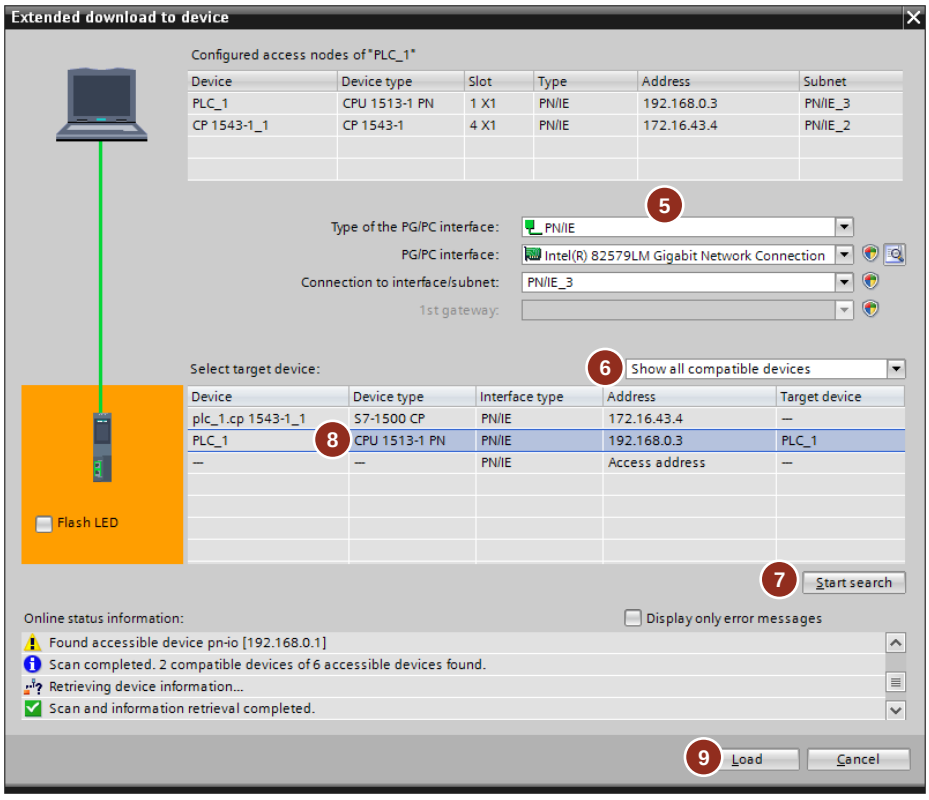
If your S7-CPU has an integrated PROFINET interface or your S7 station includes an Industrial Ethernet CP, you can download the library blocks to the S7-CPU via TCP/IP.

1. Make sure that your PG/PC and the S7-CPU are connected to the same subnet.
2. Assign the IP address you have registered in the hardware configuration to the S7-CPU.
   Note
   Alternatively, for the S7-1500 you can set the IP address on the display of the CPU.
3. Click the "Download to device" button in the project tree of the CPU to download the hardware configuration and the software to the S7-CPU. The "Extended download to device" or "Load preview" dialog box, respectively, opens automatically.

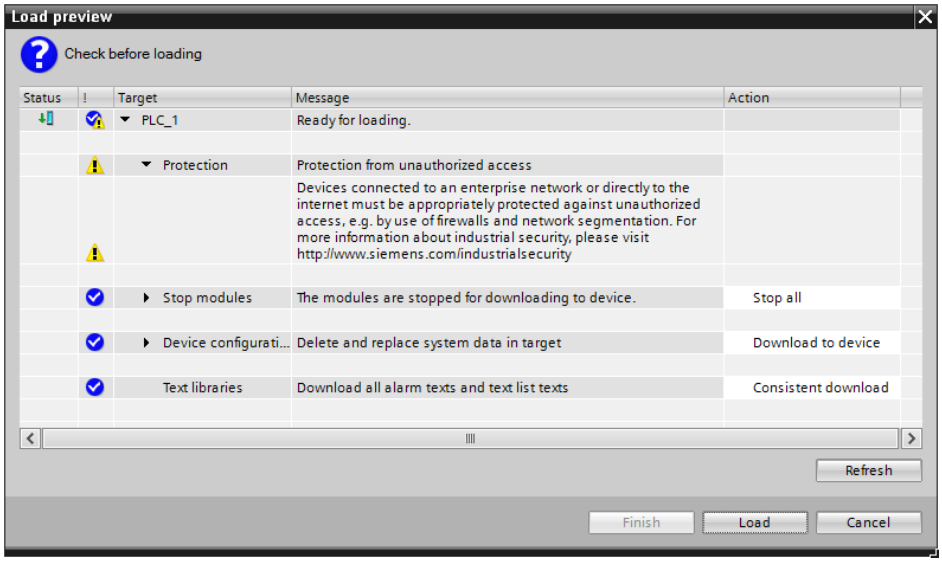


4. The "Extended download to device" dialog box only opens automatically if the access path from the PG/PC to the S7-CPU has to be reset.
5. Make the following settings in the "Extended download to device" dialog box to access the CPU via TCP/IP.
   - Type of the PG/PC interface: PN/IE
   - PG/PC interface: Network card of the PG/PC
   - Connection to interface/subnet: Subnet of the CPU, e.g. PN/IE_1
6. Select the "Show all compatible devices" option.
7. Click the "Start search" button.
8. Select the S7-CPU or the Industrial Ethernet CP as target devices.

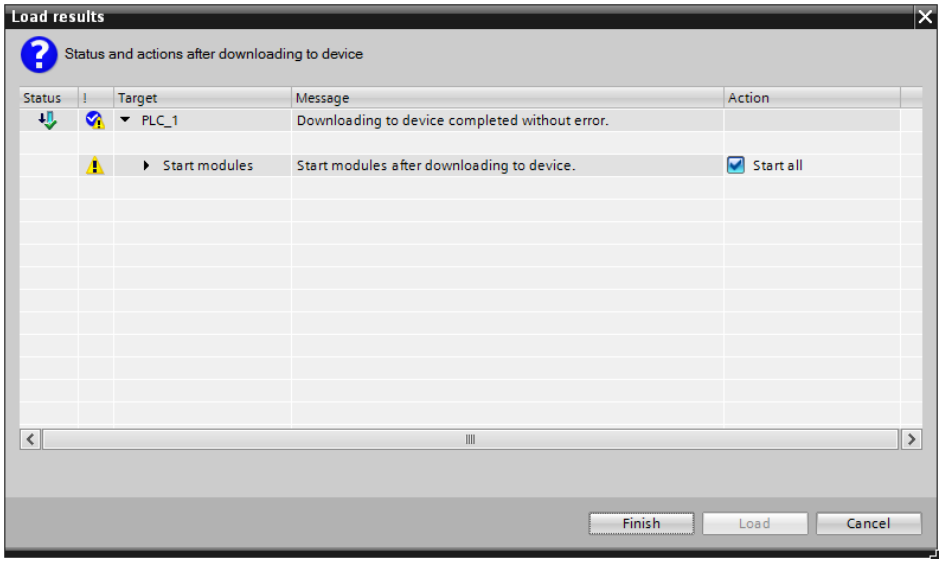
9. Click on the "Load" button.



10. Click the "Load" button in the "Load preview" dialog box to start the loading process.



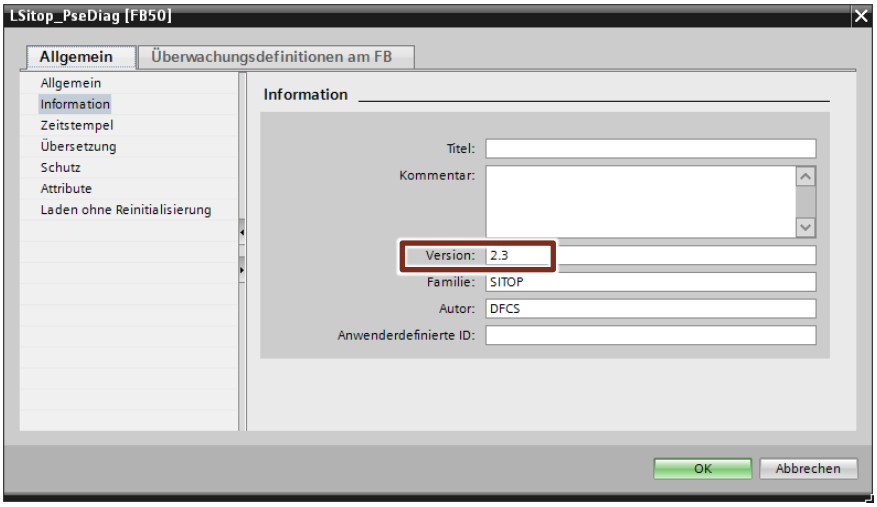
11. Click the "Finish" button in the "Load results" dialog box to exit the loading process.



2.2.4 Updating the library

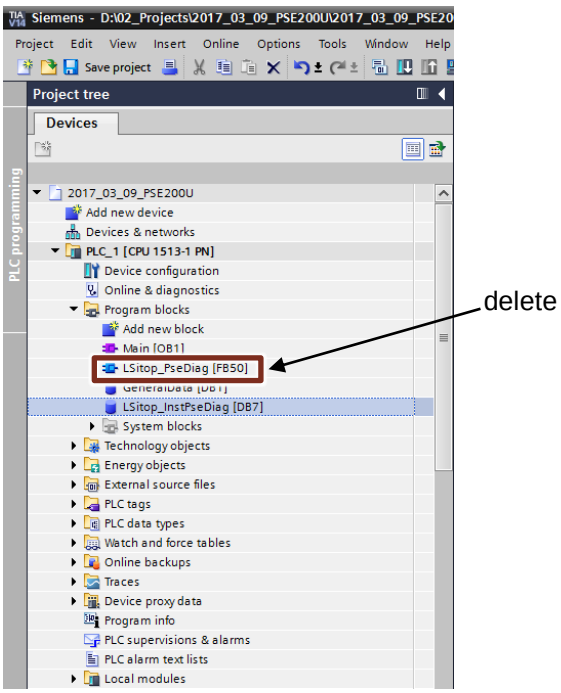
The following instructions show you how to check that the library is up-to-date and how to integrate a newer version of the LSitop library into your STEP 7 project.

1. Perform the following steps for the "LSitop_PseDiag" function block of the LSitop library.
   - Right click the "LSitop_PseDiag" function block in the project tree. Select "Properties" entry from the context menu.
   - In the displayed properties window, select the "Information" tab.
   - Compare the current version number in the "Version" output field with the latest release from Siemens Industry Online Support.



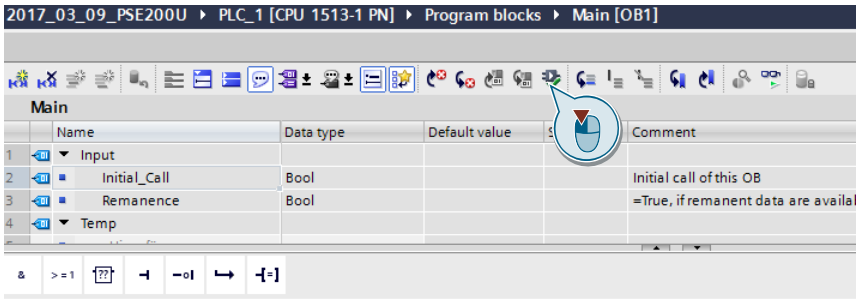
2. To update the library blocks in your STEP 7 project, integrate the latest version of the LSitop library in STEP 7 (TIA Portal) V14 (see chapter 2.2.2).

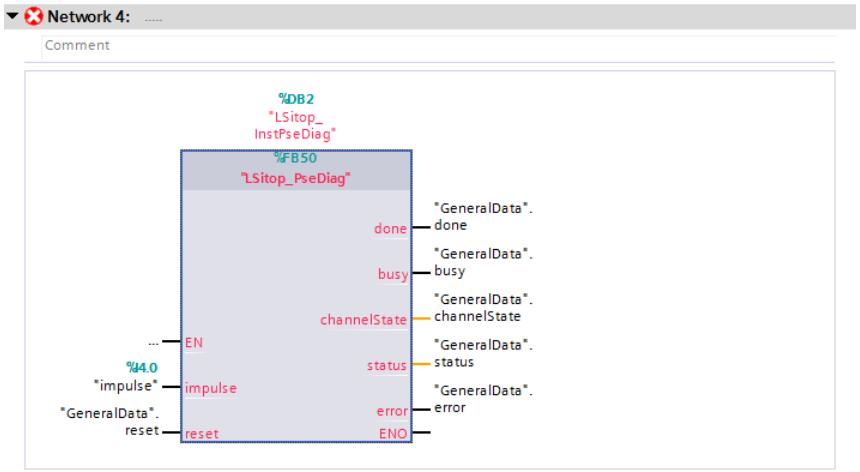
3. Delete the "LSitop_PseDiag" function block in your STEP 7 project in the "Program blocks" folder. Do not delete the function block call in the OB Main (OB1).



4. As described in chapter 2.2.2 up to step no. 3, add the latest version of the "LSitop_PseDiag" function block from the LSitop library into your STEP 7 project.

5. The updated blocks are now included in the library.
   - However, the original call of "LSitop_PseDiag" function block still indicates a missing instance data block.
   - Click the "Update inconsistent block calls" button. All instance DBs will be updated and reorganized.





2.3 Error handling

Status 16#8001

Figure 2-2 shows the graphic display of the function sequences of the "LSitop_PseDiag" function block in the event of an error, for example, when the cycle time of 100 ms is exceeded.

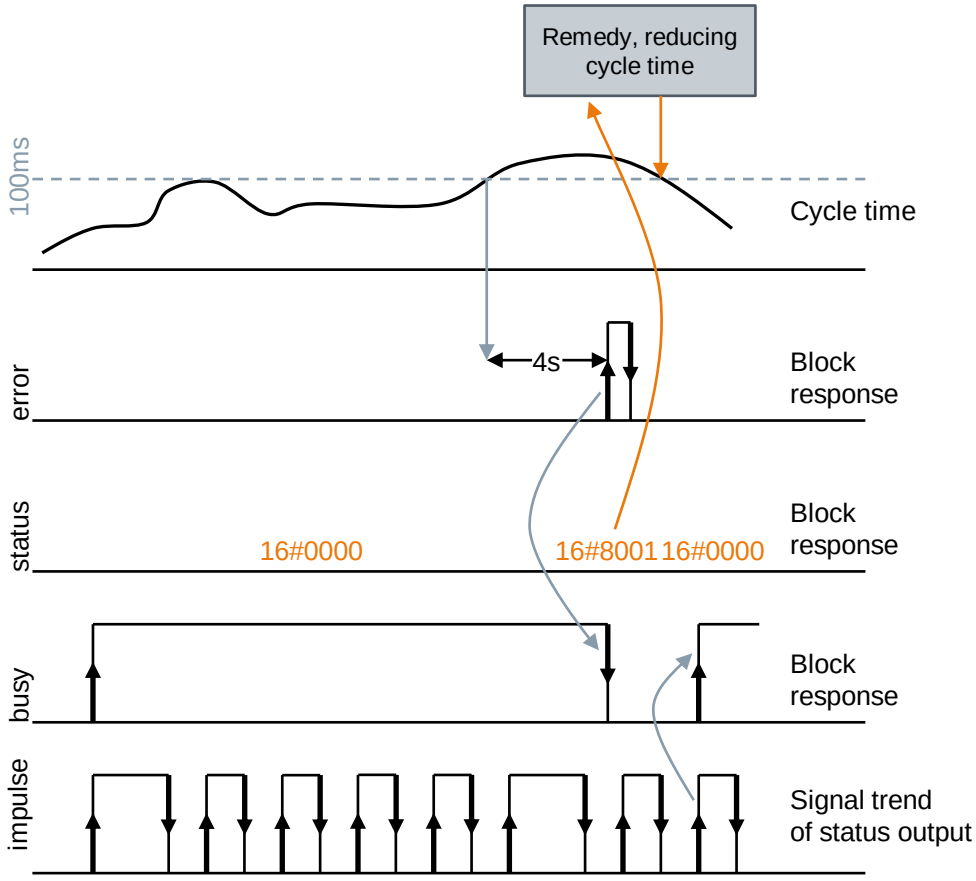
When the cycle time is longer than 4s larger than 100ms,

- the "error" output is set to TRUE for one cycle
- the value 16#8001 is output on the "status" output for one cycle.
- the "busy" output is set to FALSE

As long as the cycle time is more than 100ms, the "error" output is set to TRUE every 4 seconds for one cycle, and the value 16#8001 is output on the "status" output.

The "busy" output is only set to TRUE again when the cycle time is less than 100ms and a signal change is detected on the "impulse" input.

Figure 2-2



Status 16#8002

Figure 2-3 shows the graphic display of the functional sequences of the "LSitop_PseDiag" function block in the event of an error, for example, if the selectivity module is defective and does not provide a signal on the status output. Therefore, there will be no signal change on the "impulse" input of the "LSitop_PseDiag" function block.

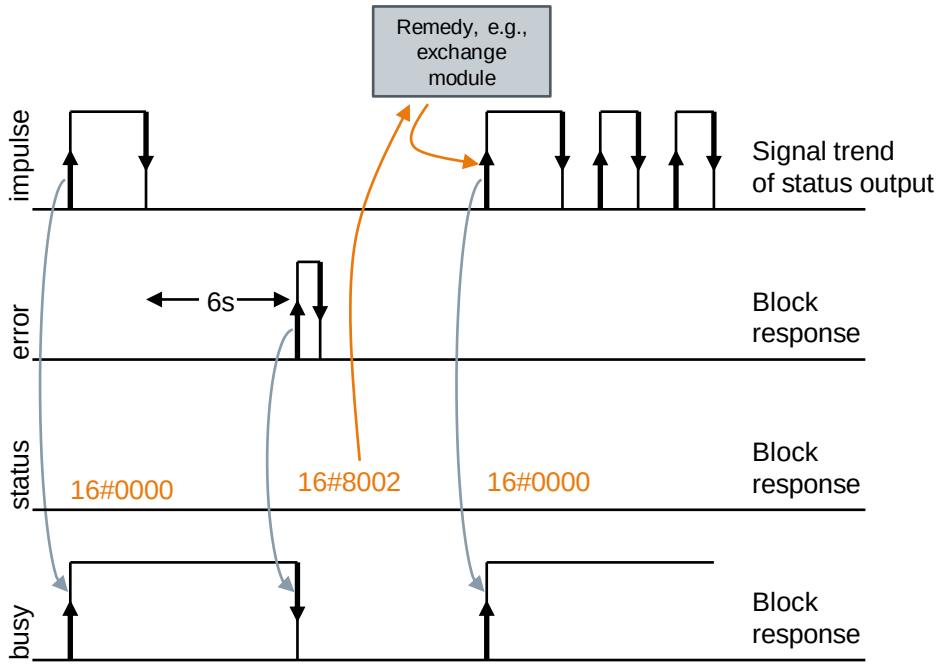
If the signal change fails to appear for more than 6 seconds:

- the "error" output is set to TRUE for one cycle
- the value 16#8002 is output on the "status" output for one cycle.
- the "busy" output is set to FALSE.

As long as the "LSitop_PseDiag" function block does not detect a signal change on the "impulse" input, the "error" output is set to TRUE every 6 seconds for one cycle, and the value 16#8002 is output at the "status" output.

The "busy" output is only set to TRUE again when a signal change is detected on the "impulse" input.

Figure 2-3



3 Valuable Information

3.1 Time synchronization

3.1.1 Procedure for time synchronization

NTP procedure

For the NTP procedure the CP or the CPU sends time requests to one or several NTP servers in the subnet (LAN). Based on the replies of the server, the most reliable and precise time is detected and the time of the requesting module is synchronized. Possible received MMS clock messages are ignored in this case.

In general, the UTC (Universal Time Coordinated) is transferred in the NTP procedure. This corresponds to GMT (Greenwich Mean Time).

The advantage of this procedure is the possible time synchronization across subnet boundaries.

SIMATIC procedure

For the SIMATIC procedure the time is set according to MMS time messages (MMS- Manufacturing Message Specification). MMS time messages are from a SIMATIC clock transmitter or a CPU that is configured as time master.

For a CP the time messages can either be received by the local CPU or via LAN. It can be set whether the CP is to pass on the received time.

In comparison to a NTP procedure that may be available, the SIMATIC procedure provides higher precision.

3.1.2 Effect of the time synchronization to the "LSitop_PSeDiag" function block in S7-1200

In S7-1200 the TIME_TCK instruction for reading the system time does not exist. Since the time is used for calculating the cycle time and the length of the pulses and pauses in the "LSitop_PSeDiag" function block for the S7-1200, the "channelState" output must not be evaluated during the time synchronization. By setting the time, the calculated cycle time and length of pulses and pauses may be incorrect in the first frame after time synchronization.

4 Appendix

4.1 Service and Support

Industry Online Support

Do you have any questions or need support?

Siemens Industry Online Support offers access to our entire service and support know-how as well as to our services.

Siemens Industry Online Support is the central address for information on our products, solutions and services.

Product information, manuals, downloads, FAQs and application examples – all information is accessible with just a few mouse clicks at
https://support.industry.siemens.com

Technical Support

Siemens Industry's Technical Support offers quick and competent support regarding all technical queries with numerous tailor-made offers
– from basic support to individual support contracts.

Please address your requests to the Technical Support via the web form:
www.siemens.en/industry/supportrequest

Service offer

Our service offer comprises, among other things, the following services:

- Product Training
- Plant Data Services
- Spare Parts Services
- Repair Services
- On Site and Maintenance Services
- Retrofit & Modernization Services
- Service Programs and Agreements

Detailed information on our service offer is available in the Service Catalog:
https://support.industry.siemens.com/cs/sc

Industry Online Support app

Thanks to the "Siemens Industry Online Support" app, you will get optimum support even when you are on the move. The app is available for Apple iOS, Android and Windows Phone:
https://support.industry.siemens.com/cs/ww/en/sc/2067

4.2 Links and Literature

Table 4-1

No.	Topic
\1\	Siemens Industry Online Support https://support.industry.siemens.com
\2\	Link to the entry page of the application example https://support.industry.siemens.com/cs/ww/en/view/61450284
\3\	

4.3 Change documentation

Table 4-2

Version	Date	Modifications
V1.0	07/2013	First version
V2.0	06/2016	Library description summarized for all CPU types
V3.0	03/2017	• Structure of library description changed • Modification in the library description due to changes in programming of the "LSitop_PseDiag" function block