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# Function Block for Monitoring 24V Load Circuits

SITOP PSE200U, STEP 7 V5.5

<https://support.industry.siemens.com/cs/ww/en/view/61450284>

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# 1 Introduction

## 1.1 Overview

The SITOP PSE200U electronic selectivity module is designed to be connected to a controlled 24V DC power supply with up to 40 A output current. The selectivity module splits the 24 V DC output voltage generated by a controlled power supply between four load circuits. For each output, the rated current can be set individually with a potentiometer in the range from 0.5 A to 3A or from 3 A to 10A, respectively, depending on the type. If the rated current exceeds these values, the output will be disabled after a certain period of time and can be re-enabled using buttons on the selectivity module or via remote reset after a certain waiting time has elapsed.

## 1.2 Mode of operation

The status output (S) of the selectivity module supplies a signal that serially codes the state of the 4 load circuits.

The signal of status output (S) of the S7-CPU is read and evaluated via a digital input. This allows you to monitor the status of outputs 1 to 4 via the application program of the S7-CPU.

The S7-CPU detects, whether the consumer connected to output 1, e.g. a motor, has produced an overload.

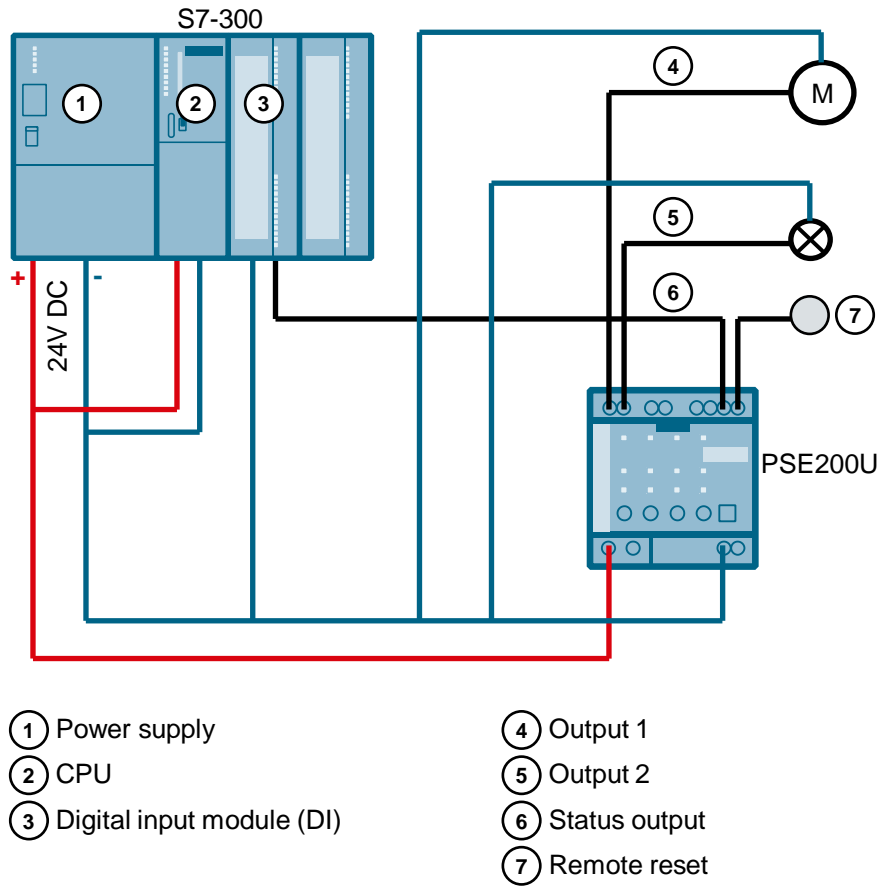
The S7 CPU detects, whether the consumer connected to output 2, e.g., a light, has produced a short-circuit.



### 1.2.1 Application with S7-300/S7-400

The following figure shows the monitoring of 24V load circuits by the selectivity module SITOP PSE200U and S7-300/S7-400 CPU.

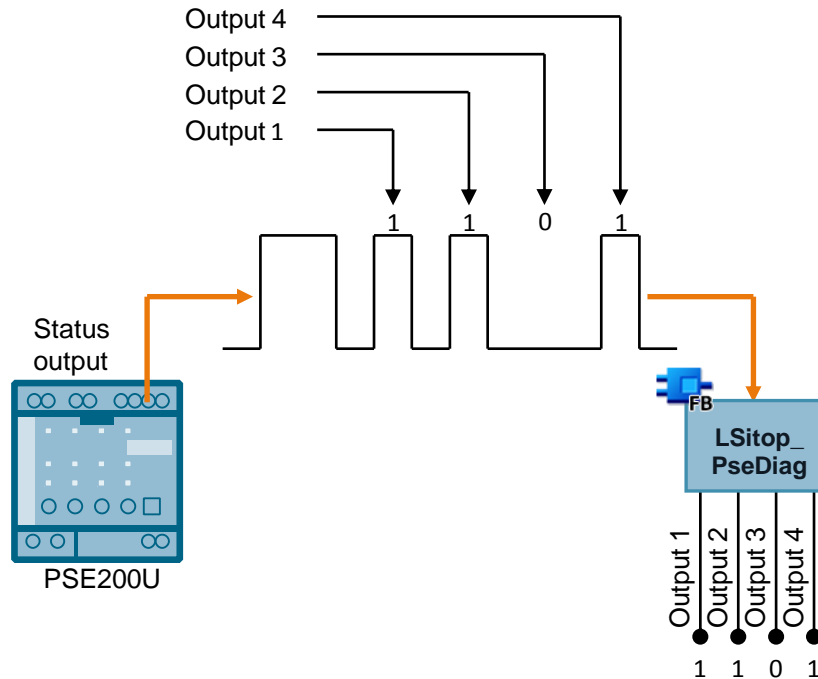
Figure 1-1



### 1.2.2 Workflow

The LSitop library supplies the "LSitop\_PseDiag" function for S7-300/S7-400 CPUs. Call the "LSitop\_PseDiag" function block in the user program of the S7-CPU in order to evaluate the signal of the status output (S). The "LSitop\_PseDiag" function block reads the signal of the status output (S) via an input and displays the state of the four outputs of the selectivity module on its output.

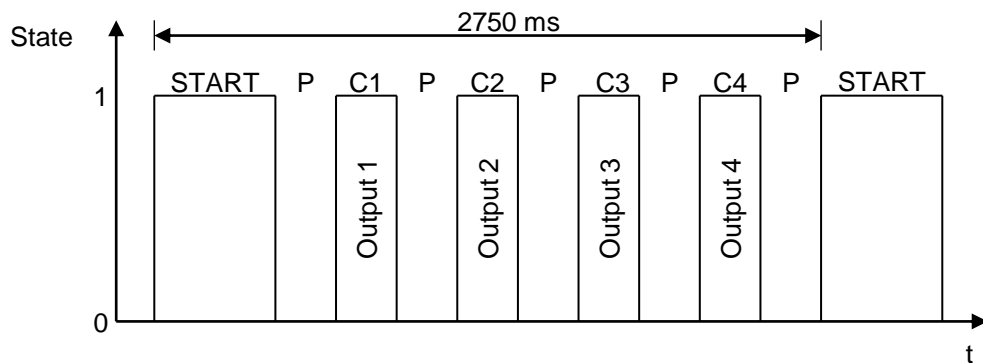
Figure 1-2



### 1.2.3 Signal trend of the status output (S)

Figure 1-3 shows the signal trend of the status output (S). A message of the signal consists of one start bit and four channel bits that are separated each by a pause bit. The start bit is always "1" and the pause bits are always "0". The channel bits signal the state of the outputs 1 thru 4.

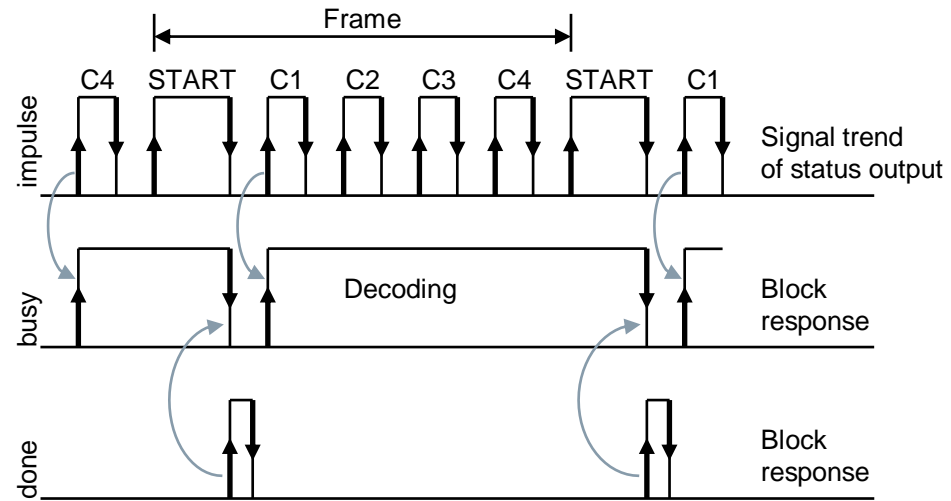
Figure 1-3



### 1.2.4 Functional sequences of the "LSitop\_PseDiag" function block

Figure 1-4 shows the graphic representation of the functional sequence of the "LSitop\_PseDiag" function block.

Figure 1-4



### 1.2.5 Internally used system functions for S7-300/S7-400 CPUs

For the S7-300/S7-400 CPUs the following instructions are called internally in the "LSitop\_PseDiag" function block:

- **TIME\_TCK (SFC 64):** The TIME\_TCK (SFC 64) system function reads the system time from the CPU. The system time is a time counter that counts from 0 to max. 2147483647ms. If an overflow occurs, counting is started again at "0". The time grid and the precision of the system time is 1ms.  
The system time is used in the "LSitop\_PseDiag" function block to calculate the cycle time as well as the length of the pulses and pauses.  
The TIME\_TCK (SFC 64) system function can be found in the standard library in the "System Function Blocks > Blocks" folder:
- **TON (SFB 4):** The TON (SFB 4) system function block is used to generate a switch-on delay. The switch-on delay is used for the generation of the error messages in the "LSitop\_PseDiag" function block.  
The TON (SFB 4) system function can be found in the standard library in the "System Function Blocks > Blocks" folder:

#### Comparing time values

To calculate the cycle time and the length of the pulses and pauses, the read system time must be higher than the time read and saved in the last cycle. This means that relational expressions are used in the function block to compare for higher values of the contents of two variables of TIME data type.

#### Calculating cycle time

To calculate the cycle time, the system time read in every cycle is saved and subtracted from the newly read system in the next cycle. The cycle time may be max. 100 ms so that each pulse can be detected in the signal trend of the status output (S). If the cycle time exceeds 100 ms, the "LSitop\_PseDiag" function block will output an error with the value 16#8001 on the "status" output.

#### Calculating the length of a pulse

In order to calculate the length of a pulse, the system time is read and saved when a positive edge is detected on the "impulse" input. When a negative edge is subsequently detected, the system time is read and saved again. The system time saved for a positive edge is subtracted from the saved system time for a negative edge.

#### Calculating the length of a pause

In order to calculate the length of a pause, the system time is read and saved when a negative edge is detected on the "impulse" input. When a positive edge is subsequently detected, the system time is read and saved again. The system time saved for a negative edge is subtracted from the saved system time for a positive edge.



### 1.2.6 Mode of operation of the selectivity module

A multi-color LED display at the device front indicates the operating state of the related outputs.

Table 1-1 shows which mode has the effect that outputs 1 to 4 switch to state 0 or 1, respectively, during the signal trend of the status output (S).

Table 1-1

| LED displays     | Mode   | Status output 1 to 4  |
|------------------|--|---|
| off              | All LED displays: <ul style="list-style-type: none"> <li>Supply voltage missing</li> <li>Start-up of the device: Once the start-up of the device is accomplished, the outputs will be switched on whilst considering the set connect delay.</li> </ul> | During startup or when the supply voltage is missing there will be no signaling on the status output. The status is continuously 0. |
|                  | LED display of individual output: <ul style="list-style-type: none"> <li>Output defective (internal fuse has tripped)</li> </ul>   | 0   |
| Lights up green  | Normal operation, output connected   | 1   |
| Flashing green   | Overload on output: Output current 101 to 150% of response threshold (admissible for 5s)   | 1   |
| Lights up red    | Output switched off due to overload  | 0   |
| Flashing red     | Output ready for reset of automatic switch-off by clicking the button on the selectivity module or the remote reset (effective for all automatically switched off outputs)   | 0   |
| Flashing orange  | Output manually switched off by clicking a button on the selectivity module: The state is saved when the device is switched off and can only be reset by pressing the button again.  | 0   |
| Red chaser light | Excessive temperature of device: Once the excessive temperature has cooled down, the outputs can be switched on again.   | 0   |

## 1.3 Components used

This application example was created with the following hardware and software components:

Table 1-2

| Component   | Number | Article number     | Alternative  |
|---|--------|--------------------|--|
| SITOP PSE200U 3A with single-channel signaling (selectivity module) | 1      | 6EP1961-2BA31      | <ul style="list-style-type: none"> <li>SITOP PSE200U 10A, article number: 6EP961-2BA41</li> <li>SITOP PSE200U 3A NEC Class 2, article number: 6EP961-2BA51 6EP961-2BA61</li> </ul> |
| S7-CPU  | 1      | 6ES7315-2EH14-0AB0 | <ul style="list-style-type: none"> <li>Any S7-300/S7-400 CPU</li> <li>IM 151-8(F) PN/DP CPU</li> <li>IM 154-8(F/FX) PN/DP CPU</li> </ul>   |
| DI 8/DO 8x24VDC/0.5A  | 1      | 6ES7323-1BH01-0AA0 | Other digital input modules and digital output modules   |
| STEP 7 V5.5 SP4   | 1      | 6ES7810-4CC10-0YA5 | For the configuration of the S7-CPU you require STEP 7 V5.5 SP4 or higher.   |

## 2 Engineering

### 2.1 Interface description

The "LSitop\_PseDiag" function block reads the status output (S) via the "impulse" input of the selectivity module in order to evaluate the signal trend of the status output (S) and to display the state of outputs 1 to 4 on the "channelState" output.

Figure 2-1 shows the call of the "LSitop\_PseDiag" function block in the user program.

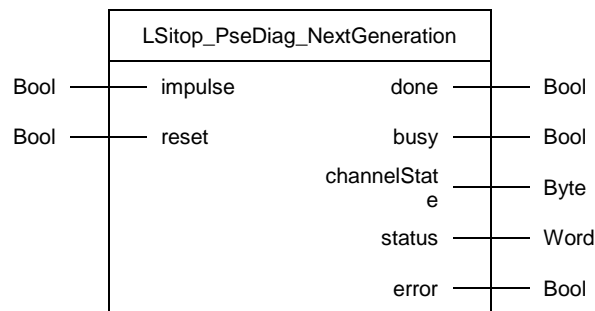
Call the "LSitop\_PseDiag" function block in the user program of the S7-CPU cyclically in OB1 or in an interrupt OB with max. 100 ms.

The cycle time may be max. 100 ms so that each pulse is detected in the signal trend of the status output (S).

#### Note

If the cycle time exceeds 100 ms, the "LSitop\_PseDiag" function block will output an error with the value 16#8001 on the "status" output.

Figure 2-1



The following table shows the parameters of the "LSitop\_PseDiag" function block.

Table 2-1

| Name    | P type | Data type | Comment   |
|---------|--------|-----------|---|
| impulse | IN     | Bool      | Input via which the signal of the status output of the selectivity module is read.<br>Figure 1-3 shows the signal trend of the status output (S). |
| reset   | IN     | Bool      | A reset is tripped on positive edge. All parameters (static variables and outputs of the "LSitop_PseDiag" function block) are reset.              |

| Name         | P type | Data type | Comment  |
|--------------|--------|-----------|--|
| done         | OUT    | Bool      | done = 1: A frame was evaluated completely and without error. The state of outputs 1 to 4 of the selectivity module is displayed on the "channelState" output. The data of the "channelState" output can be accepted. The value done = 1 is set for one cycle.<br>done = 0: Frame evaluation is running or no signal detected on "impulse" input.  |
| busy         | OUT    | Bool      | busy = 1: Function block "LSitop_PseDiag" is active<br>busy = 0: If done = 1 a frame was evaluated completely and without error. The state of outputs 1 to 4 of the selectivity module is displayed on the "channelState" output. The data of the "channelState" output can be accepted.   |
| channelState | OUT    | Byte      | Status of outputs 1 to 4<br>Bit 0 = 1 if output 1 has status 0<br>Bit 0 = 0 if output 1 has status 1<br>Bit 1 = 1 if output 2 has status 0<br>Bit 1 = 0 if output 2 has status 1<br>Bit 2 = 1 if output 3 has status 0<br>Bit 2 = 0 if output 3 has status 1<br>Bit 3 = 1 if output 4 has status 0<br>Bit 3 = 0 if output 4 has status 1<br>Bit 4: not assigned<br>Bit 5: not assigned<br>Bit 6: not assigned<br>Bit 7: not assigned<br><a href="#">Table 1-1</a> gives an overview of the modes and the status of outputs 1 to 4. |
| status       | OUT    | Word      | Status indication:<br>If error = 1 the error code for one cycle is displayed on the "status" output.<br>If error = 0 the value 16#0000 is displayed at the "status" output.  |
| error        | OUT    | Bool      | <ul style="list-style-type: none"> <li>error = 1: An error occurred during the execution of the routine. The value error = 1 is set for one cycle.</li> <li>error = 0: no error</li> </ul>   |

**Note**

The instance DB of the "LSitop\_PseDiag" function block is generated when the "LSitop\_PseDiag" function block is called up. For each call of the "LSitop\_PseDiag" function block you require an independent instance DB. The "LSitop\_PseDiag" function block must not be called up more than once with the same instance DB.

## Status indication

Table 2-2

| Value on the "status" output | Meaning  | Remedy/note  |
|------------------------------|--|--|
| 16#8001                      | 100 ms cycle time exceeded   | Call the "LSitop_PseDiag" function block with max. 100 ms.   |
| 16#8002                      | No signal change was detected on the "impulse" input for at least 6 s. | <ul style="list-style-type: none"> <li>Check whether the status output (S) of the selectivity module is connected to the digital input.</li> <li>Check whether you specified the correct digital input on the "impulse" input.</li> <li>Check if the power supply is connected to the selectivity module.</li> </ul> |

## 2.2 Integration into the user project

Below, you will find the steps necessary for opening the LSitop library in STEP 7 and how to integrate it in your STEP 7 project. After the integration process is complete you can make use of the function blocks of the LSitop library.

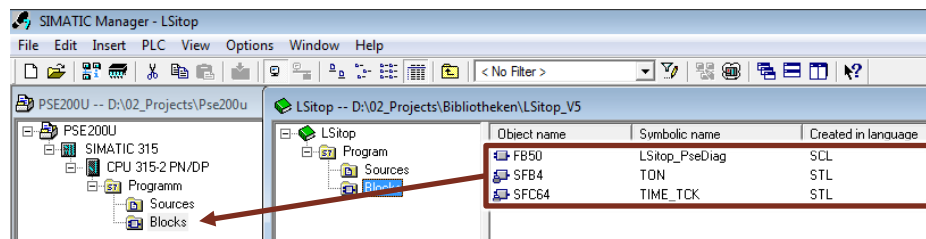
### Note

In the following section it is assumed that a STEP 7 project has been created.

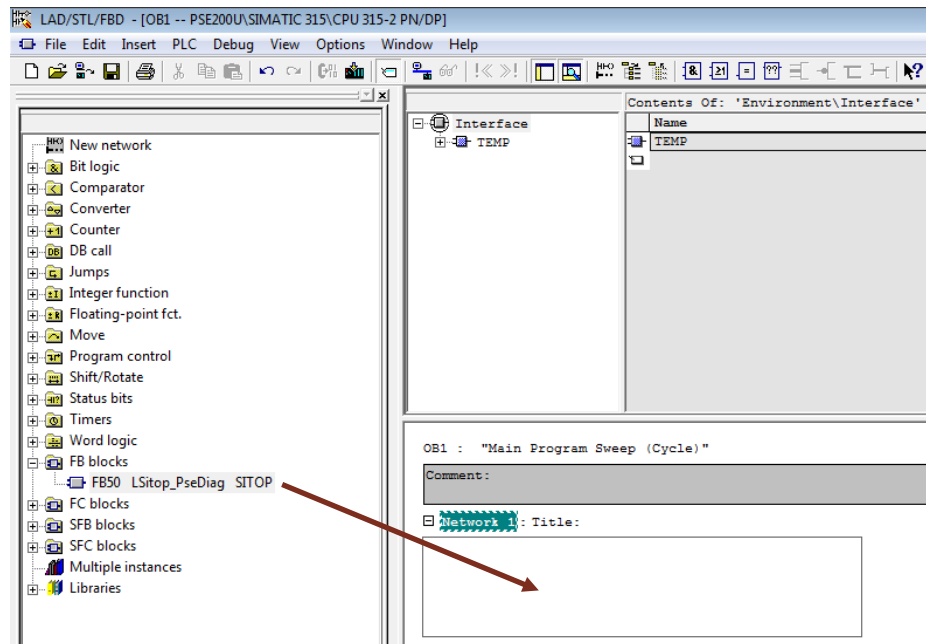
1. The library is available on the HTML page from which you downloaded this document. Save the "61450284\_PSE200U\_STEP7\_V5\_LIB\_V23.zip" library on your hard drive.
2. Unzip the library.
3. Open the SIMATIC Manager.
4. Select the menu "File > Open".
5. Select the LSitop library in the "Library" tab and click the "OK" button to open the LSitop library.

### 2.2.1 Integrating the library blocks into the STEP 7 project

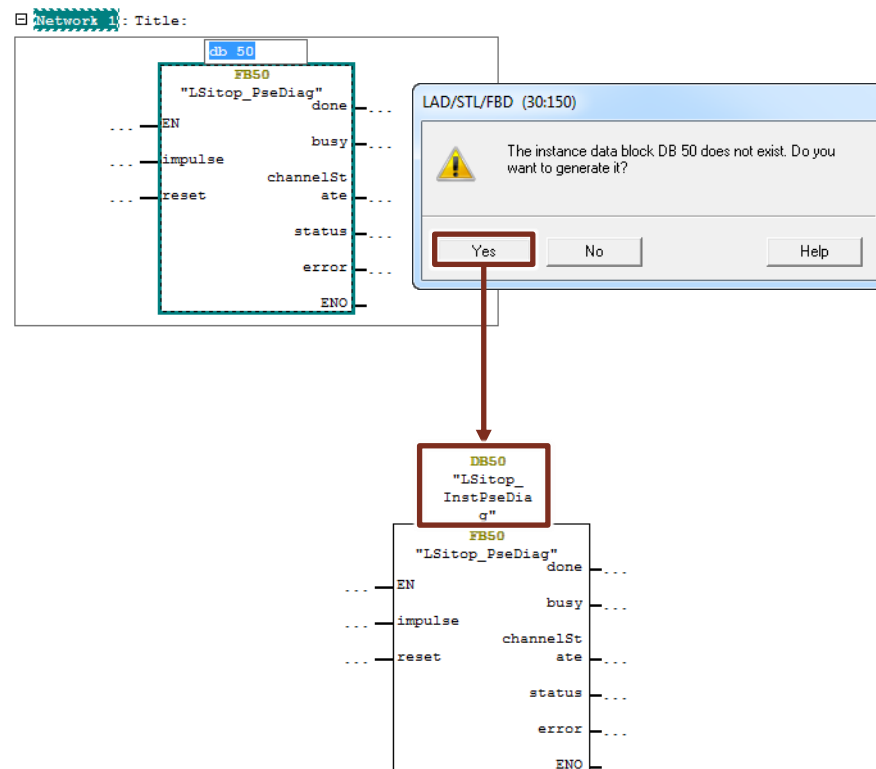
1. Once you have opened the LSitop library, open your STEP 7 project.
2. Copy the blocks of the LSitop library into your STEP 7 project. To do so, select all the blocks in the library's block folder and move it into the block folder of your STEP 7 project using drag-and-drop.



3. Create the OB1 organization block. Open it and move the "LSitop\_PseDiag" function block into any network via drag-and-drop.



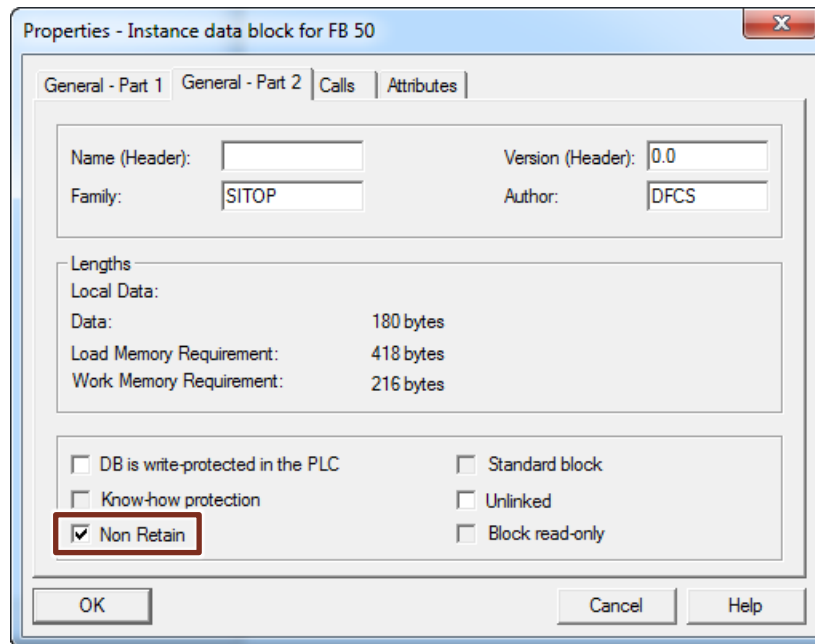
4. Select the related instance data block. If the instance data block does not exist, it has to be generated.



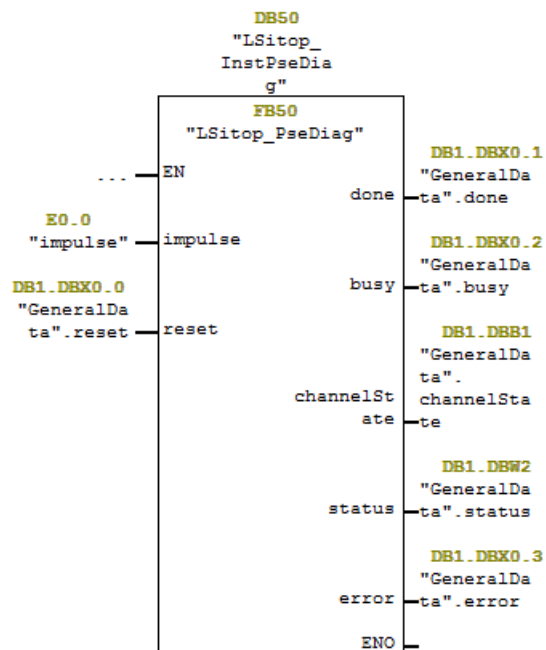
5. Right-click the new instance data block in the program block folder, and select the option "Object Properties" from the context menu to open the properties dialog box of the instance data block.



6. Enable the "Non Retain" option in the "General - Part 2" tab to overwrite the instance DB with the initial values on CPU restart.



7. Assign values to all the necessary formal parameters.



8. Save and close the organization block OB1.

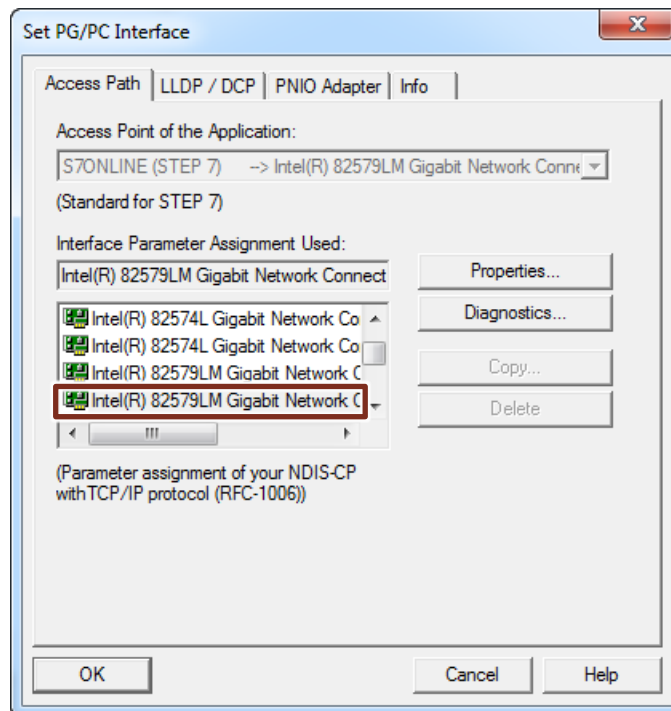
### 2.2.2 Downloading the library blocks to the S7-CPU

Below you will find the steps necessary to download all the blocks of your application program to the S7-CPU.

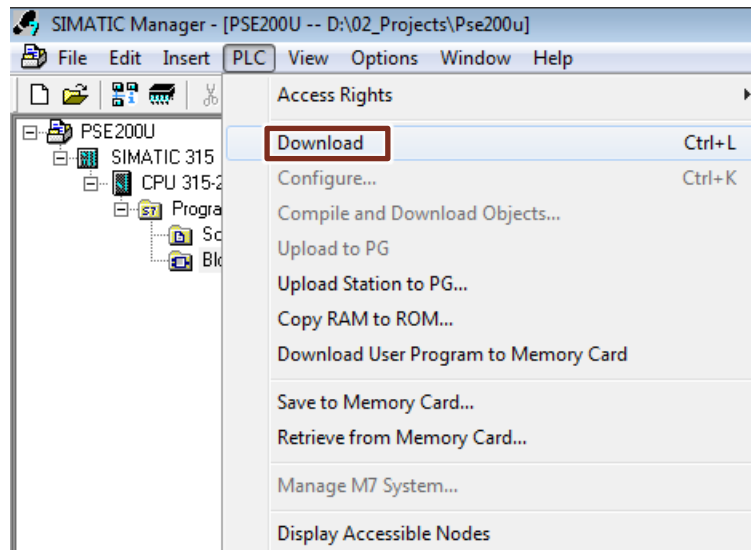
#### Downloading via TCP/IP

If your S7-CPU has an integrated PROFINET interface or your S7 station includes an Industrial Ethernet CP, you can download the library blocks to the S7-CPU via TCP/IP.

1. Make sure that your PG/PC and the S7-CPU are connected to the same subnet.
2. Select the "Options > Set PC/PG Interface" menu in the SIMATIC Manager in order to set the PG/PC interface to TCP/IP.



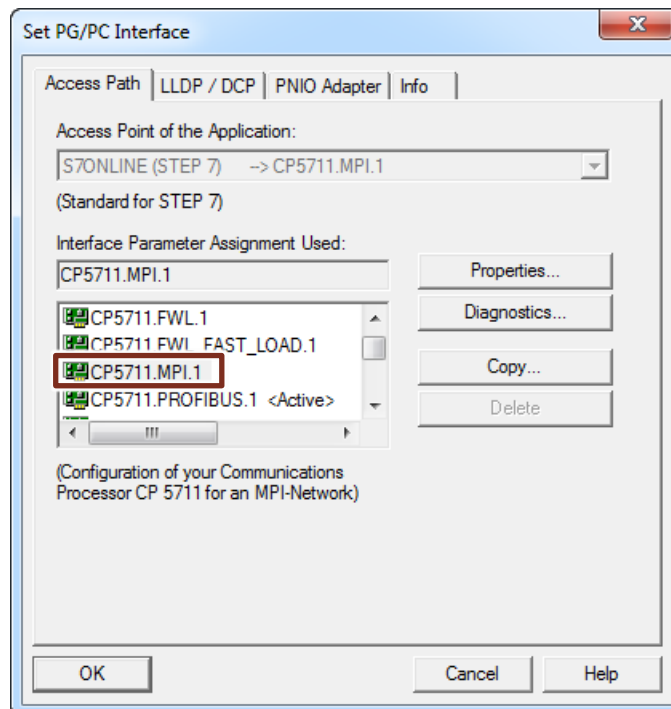
3. Select the S7 station and select the “PLC > Download” menu in order to load the whole project to your CPU.



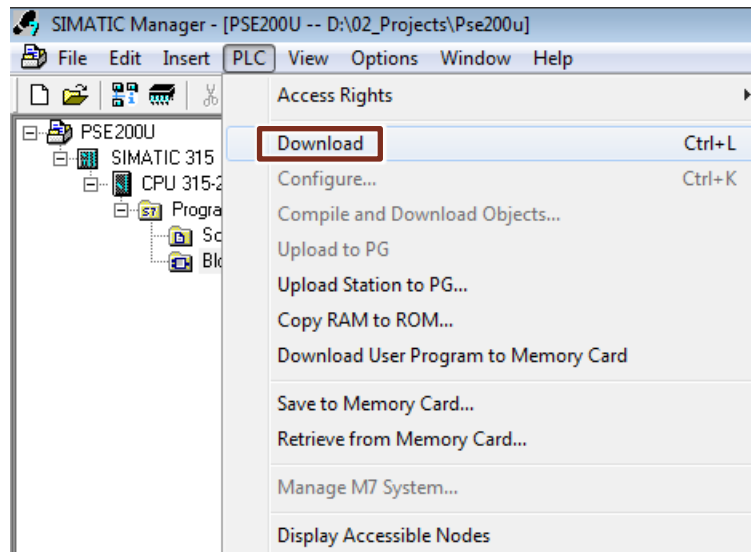
### Downloading via MPI

You can also download the blocks to the S7-300/S7-400 via the MPI or MPI/DP interface.

1. Connect the PC/PG to the MPI or MPI/DP interface of the S7-300/S7-400 CPU using a PROFIBUS bus cable or an MPI cable.
2. Select the “Options > Set PG/PC Interface” menu in the SIMATIC Manager in order to set the PG/PC interface to MPI.
3. Set the appropriate access path, for example, CP5711.MPI.1 in the “Set PG/PC Interface” dialog box. Apply the settings with “OK”.



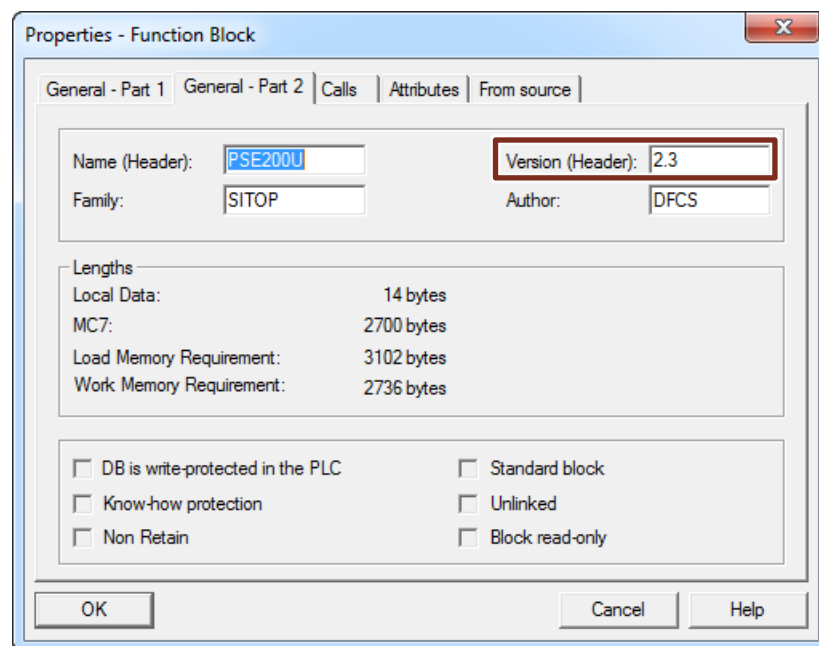
4. Select the S7 station and select the “PLC > Download” menu in order to load the whole project to your CPU.



### 2.2.3 Updating the library

The following instructions show you how to check that the library is up-to-date and how to integrate a newer version of the LSiTop library into your STEP 7 project.

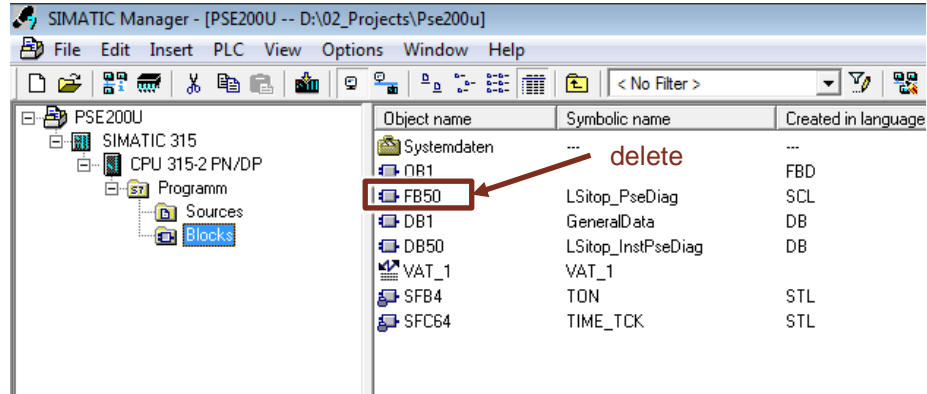
1. Perform the following steps for the "LSiTop\_PseDiag" function block of the LSiTop library.
  - Right-click the function block and select the “Object Properties” option in the context menu. The properties dialog of the function block opens.
  - Compare the current version number in the “Version” output field with the latest release from Siemens Industry Online Support in the “General – Part 2”.



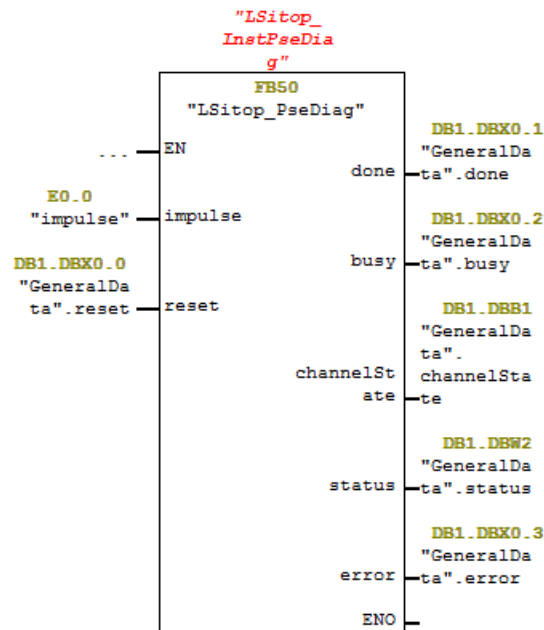
2. To update the library blocks in your STEP 7 project, integrate the latest version of the LSiTop library in STEP 7 (see chapter 2.2.1).
3. Delete all the blocks of the library in the "Blocks" folder of your STEP 7 project.

**Note**

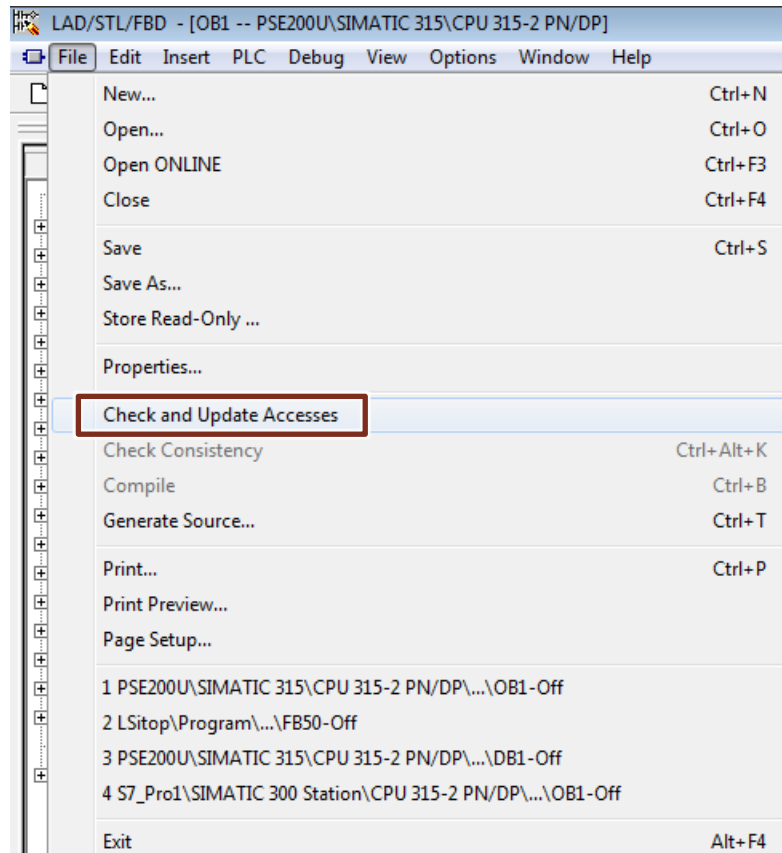
Do not delete the function block call in OB1.



4. Add the latest version of the LSiTop library blocks into your STEP 7 project following the instructions in 2.2.1 up to step 3.
5. The updated blocks are now included in the library. However, the original call of "LSitop\_PseDiag" function block still indicates a missing instance data block.



6. Select the “Check and Update Accesses” menu to check all operands for type compatibility and highlight them in red in the case of an error. All instance DBs will be updated and reorganized.





## 2.3 Error handling

### Status 16#8001

Figure 2-2 shows the graphic display of the function sequences of the "LSitop\_PseDiag" function block in the event of an error, for example, when the cycle time of 100 ms is exceeded.

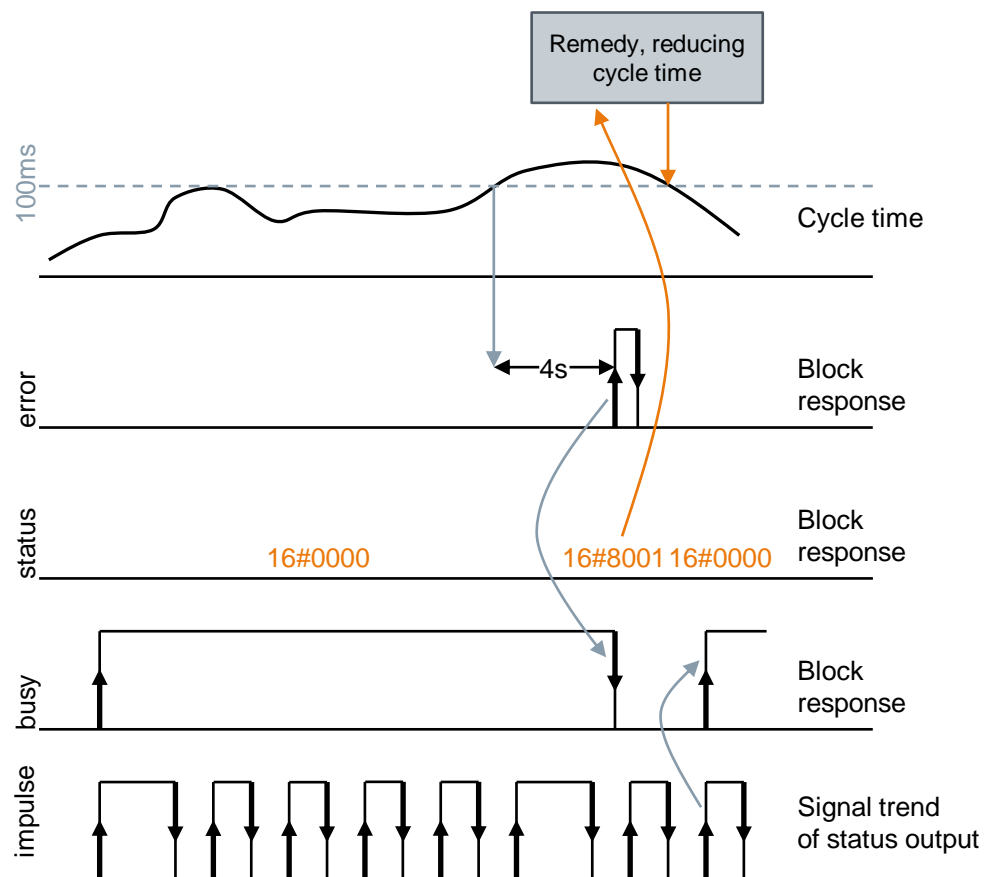
When the cycle time is longer than 4s larger than 100ms,

- the "error" output is set to TRUE for one cycle
- the value 16#8001 is output on the "status" output for one cycle.
- the "busy" output is set to FALSE

As long as the cycle time is more than 100ms, the "error" output is set to TRUE every 4 seconds for one cycle, and the value 16#8001 is output on the "status" output.

The "busy" output is only set to TRUE again when the cycle time is less than 100ms and a signal change is detected on the "impulse" input.

Figure 2-2



**Status 16#8002**

Figure 2-3 shows the graphic display of the functional sequences of the "LSitop\_PseDiag" function block in the event of an error, for example, if the selectivity module is defective and does not provide a signal on the status output. Therefore, there will be no signal change on the "impulse" input of the "LSitop\_PseDiag" function block.

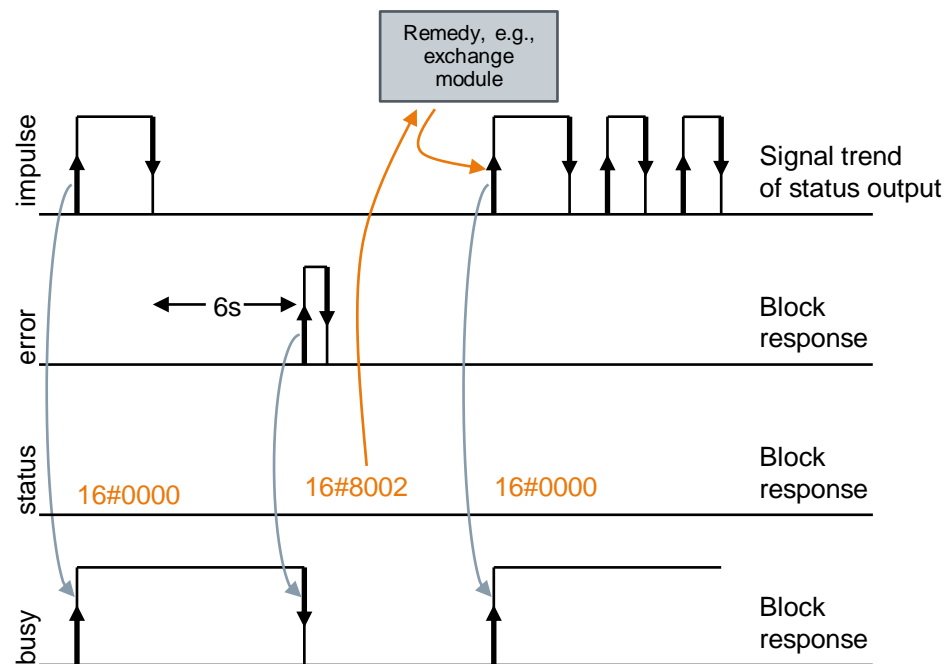
If the signal change fails to appear for more than 6 seconds:

- the "error" output is set to TRUE for one cycle
- the value 16#8002 is output on the "status" output for one cycle.
- the "busy" output is set to FALSE.

As long as the "LSitop\_PseDiag" function block does not detect a signal change on the "impulse" input, the "error" output is set to TRUE every 6 seconds for one cycle, and the value 16#8002 is output at the "status" output.

The "busy" output is only set to TRUE again when a signal change is detected on the "impulse" input.

Figure 2-3



## 3 Appendix

### 3.1 Service and Support

#### Industry Online Support

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- Spare Parts Services
- Repair Services
- On Site and Maintenance Services
- Retrofit & Modernization Services
- Service Programs and Agreements

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<https://support.industry.siemens.com/cs/sc>

#### Industry Online Support app

Thanks to the "Siemens Industry Online Support" app, you will get optimum support even when you are on the move. The app is available for Apple iOS, Android and Windows Phone:

<https://support.industry.siemens.com/cs/ww/en/sc/2067>

## 3.2 Links and Literatur

Table 3-1

| No. | Topic  |
|-----|--|
| \1\ | Siemens Industry Online Support<br><a href="https://support.industry.siemens.com">https://support.industry.siemens.com</a>   |
| \2\ | Link to the entry page of the application example<br><a href="https://support.industry.siemens.com/cs/ww/en/view/61450284">https://support.industry.siemens.com/cs/ww/en/view/61450284</a> |

## 3.3 Change documentation

Table 3-2

| Version | Date    | Modifications  |
|---------|---------|--|
| V1.0    | 07/2013 | First version  |
| V2.0    | 06/2016 | Figures and wording updated<br>Chapter 2: Explanation of the blocks no longer integrated in table 2-1 but in chapters 2.2.x.   |
| V3.0    | 03/2017 | <ul style="list-style-type: none"> <li>Structure of library description changed</li> <li>Modification in the library description due to changes in programming of the "LSitop_PseDiag" function block</li> </ul> |