

DATA SHEET

Features

- **Integrated processor ARM926EJ-S**
 - 125 / 250 MHz Core Frequency
 - 16 KB Data-Cache
 - 16 KB Instruction-Cache
 - 256 KB TCM-RAM
 - 8 KB Boot ROM
 - Little Endian
- **System Bus Structure**
 - 32 Bit / 125 MHz AHB Bus
 - Multi-Layer AHB Lite with 7 Masters and 12 Slaves
 - AHB Address Range Monitoring
- **Local Bus Unit (XHIF)**
 - Allows External Master to access internal ERTEC 200P registers
 - 16 / 32-Bit Data Bus
 - 2 x 4 Paging Registers
- **Memory Controller (EMC)**
 - 8 / 16 / 32 Bit Data Bus
 - 4 chip selects
 - Supports SDRAM, SRAM, Burst Mode Flash ROM
- **Onchip Peripherals**
 - DMA Controller
 - 6 Timers
 - 2 Watchdogs
- **I/O Interfaces**
 - 2 x 2 SPI Interfaces
 - 4 UARTs
 - 1 I²C-Interface
 - One 96-bit GPIO Port
 - 1,8 / 3,3 V I/O Buffers
- **Test / Debug Functionality**
 - Boundary Scan
- **Integrated Ethernet-Phy**
 - 2 Ports
 - Supports 100Base-TX and -FX
 - Auto Cross Over
 - Auto MDIX
 - Jitter free Latency
 -
- **Package**
 - 400 Pin FPBGA
 - Size 17mm x 17 mm
 - Ball Pitch 0,8mm

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We have checked the contents of this manual for agreement with the hardware and software described. Since deviations cannot be precluded entirely, we cannot guarantee full agreement. However, the data in this manual are reviewed regularly. Necessary corrections are included in subsequent editions. Suggestions for improvement are welcomed.

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Revisions:

Version	Date	Information
1.0	04/2013	First Version
1.1	03/2014	2: "No Schmitt Trigger" changed to "CMOS" 2.1: fout / CL added. Port-Directions corrected... 2.1.1: I-Typ of CLKP_A changed 2.1.2: title adapted 2.2: GND-Pins A2 and B13 added. 2.3: Pins TMC1 and TMC2 must be connected directly to GND 2.3: recommendation for handling special function signals added 3: all voltages listed 4.1: Values for 1.8V EMC added max Voltage for 1.2V corrected 4.2: all voltages listed 4.3: splitted into Chapter 4.2, 6.3 and 6.4 5.4: maximum frequency of SPI-Interface in slave-mode corrected 6.2.1.1: Impedance -> impedance 6.2.1.2 Update Usecase "External Host" New 6.3.2: Description for external clock source 8: Power changed 9.2: Picture updated Some minor changes

1. Functional Overview

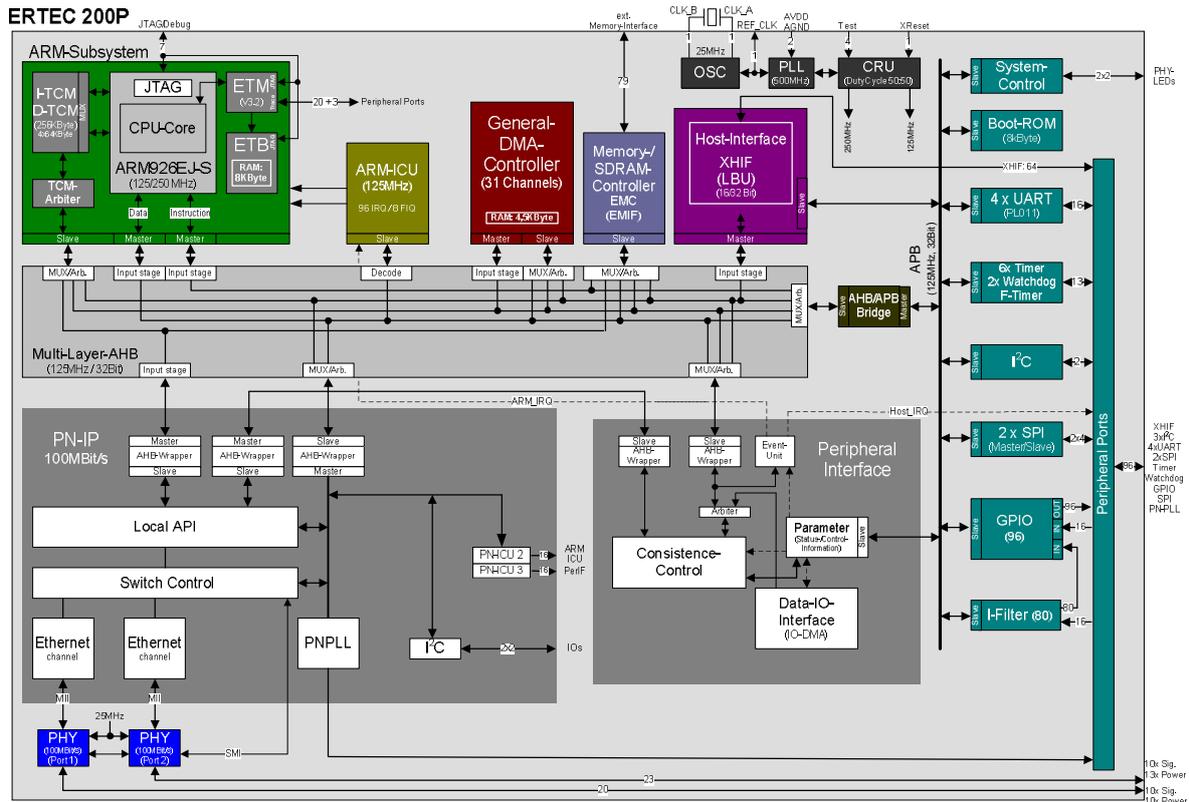


Figure 1: ERTEC 200P Blockdiagram

1.1 Key Functional Units

1.1.1 Processor Core Subsystem (ARM926)

- ARM926EJ-S Processor Core
- 8 Kbyte Boot ROM
- 256 Kbyte TCM-RAM
 - EDC with 1-Bit Error Correction and 2-Bit Error Detection, with byte access
 - configurable as Data (256-0) or Instruction (0-256)-RAM
 - configuration-step: 64 Kbyte
- ARM Interrupt Controller
 - max. 96 Interrupts
 - max. 8 fast Interrupts
 - 8 Software Interrupt inputs and 86 Hardware Interrupt inputs
- Embedded Trace Macrocell (ETM9, see /2/) for Debugging
- JTAG Block for Debugging
- Memory Management Unit (MMU) with Translation Lookaside Buffers (TLBs)
- Separate Data and Instruction-Bus

1.1.2 Processor Bus Unit

- Memory Controller (EMC)
 - SDRAM-Controller features:
 - 16 / 32 bit databus width
 - PC133 SDRAM-compatible (125 MHz synchron is used)
 - 1 Bank with max. 256 MByte SDRAM (32 Bit databus)
 - SDRAM support for following parts:
 - CAS-Latency: 2 or 3 clocks
 - Bank-address bits (1/2/4 internal banks), realized via the lowest two bits of the address bus MA(1:0)
 - 8 / 9 / 10 / 11 bits column-address MA(13), MA(11:2)
 - max. 14 bits row-address MA(15:2)
 - Asynchronous controller features:
 - 8 / 16 / 32 bit bus width (for each chip select programmable)
 - 4 chip selects
 - the timing for each chip select can be set individually
 - the response to ready signal can be set individually for each chip select
 - a maximum of 64 MByte address area for each chip select
- DMA Controller
 - 1 Channel
 - 31 Jobs
 - 20 can be started from hardware
 - 31 can be started from software
- Two SPI Interfaces
 - SPI1 via dedicated Pins
 - SPI2 via GPIO Pins
- UART Interface via dedicated Pins
- Timer Unit (Module TIMER_TOP)
 - ... reloadable Down-Counters
 - each Timer is equipped with a Multiplexer for Trigger Signals
- Interrupt Control Unit (Module ICU)
 - level or edge triggered Operation
 - 96 Interrupt Request Inputs
 - Interrupt Priority is individually selectable for each Request Input
- Watchdog Unit (Module WDG1)
 - Watchdog Interrupt Generation via Counter 0
 - Watchdog Reset Generation via Counter 1
 - Once started, the watchdog can only be stopped by a Power-On Reset.

1.1.3 PROFINET-IP (PN-IP)

- 2 Ethernet-Ports
- 100MBit/s Ethernet-Port with integrated dual PHY
- Dynamic Frame Packing
- Fast Forwarding
- Short Preamble
- Dynamic Fragmentation
- IRT-Forwarding
- PN-PLL
- Support for Synchronisation-Protocolls (PTCP)

1.1.4 Peripheral Interface (PER-IF)

- Supports Consistency for IO Data

2 Pin Description

In the signal tables, the following abbreviations are used:

Abbreviation	Description
C	CMOS Input
S	Schmitt Trigger Input
OSC	Oscillator Input
dn	Internal 50 kΩ pull-down resistor
up	Internal 50 kΩ pull-up resistor
disabled	Internal pull is disabled
PECL	Positive emitter coupled logic
bi	Bidirectional Port
AO	Analog Output
AI	Analog Input
NC	No connection
n/a	Not Applicable
-	Not Applicable

Note that signals with the prefix "X" are active low signals.

2.1 Signal Table

Hint: If no load capacitance (CL) is specified in the table, a default load of 20 pF is used.

2.1.1 Signalgroup "System"

Signal	Signaldescription	Dir	Output (V)	Input (V)	Internal Pull	Current (mA)	I-Typ	f _{out} (MHz)	CL/ MAX (pF)	pinid
REF_CLK	Reference Clock MII (ext PHY)	bi	3.3	3.3	-	6	C	25	50	W16
BYP_CLK	F-Timer Clock	in	-	3.3	-	-	C			T11
XRESET	HW-Reset	in	-	3.3	up	-	S			W15
CLKP_A ¹⁾	Quartz crystal connection	in	-	3.3	-	-	OSC			Y14
CLKP_B ¹⁾	Quartz crystal connection	out	3.3	-	-	12	-	25	50	W14

¹⁾ see Chapter 6.3.1 for recommended crystal or Chapter 6.3.2 for usage of external clock source

2.1.2 Signalgroup "Test"

Signal	Signaldescription	Dir	Output (V)	Input (V)	Pull	Current (mA)	I-Typ	f _{out} (MHz)	CL/ MAX (pF)	pinid
TEST ¹⁾	IC-Test-Mode	in	-	3.3	dn	-	S			R9
TMC1 ¹⁾	Testmode_1	in	-	3.3	-	-	C			F12
TMC2 ¹⁾	Testmode_2	in	-	3.3	-	-	C			R14
CTRL_STBY0	Stby for 3V3 GPIO(31:0)	in	-	3.3	up	-	S			M15
CTRL_STBY1	Stby for 1V8/3V3 GPIO(95:32)/XHIF	in	-	1.8/3.3	up	-	S			J15
CTRL_STBY2	Stby for 1V8/3V3 GPIO(95:32)/XHIF	in	-	1.8/3.3	up	-	S			F9
TACT ¹⁾	TESTACT-TAP-RESET	in	-	3.3	dn	-	S			R12

¹⁾ see Table 2 how to use this pin

2.1.3 Signalgroup "PHY"

Signal	Signaldescription	Dir	Output (V)	Input (V)	Internal Pull	Current (mA)	I-Typ	fout (MHz)	CL/ MAX (pF)	pinid
L_PHY_1	Link Status PHY 1	out	3.3	-	-	8	-	0.1	20	U20
A_PHY_1	Activity Status PHY 1	out	3.3	-	-	8	-	0.1	20	T13
L_PHY_2	Link Status PHY 2	out	3.3	-	-	8	-	0.1	20	U19
A_PHY_2	Activity Status PHY 2	out	3.3	-	-	8	-	0.1	20	T12
P2RXN	Port2 differential receive input	bi	AO	AI	-	18	-	62,5	n/a ¹⁾	N20
P2RXP	Port2 differential receive input	bi	AO	AI	-	18	-	62,5	n/a ¹⁾	N19
P2TXN	Port2 differential transmit output	bi	AO	AI	-	18	-	62,5	n/a ¹⁾	M20
P2TXP	Port2 differential transmit output	bi	AO	AI	-	18	-	62,5	n/a ¹⁾	M19
P2RDXP	Port2 FX differential receive input	in	-	3.3	-	-	PECL	-	-	W12
P2RDYN	Port2 FX differential receive input	in	-	3.3	-	-	PECL	-	-	Y12
P2TDXP	Port2 FX differential transmit output	out	3.3	-	-	12	-	62,5	30	W9
P2TDYN	Port2 FX differential transmit output	out	3.3	-	-	12	-	62,5	30	Y9
P2SDXP	Port2 FX differential SD input	in	-	3.3	-	-	PECL	-	-	W11
P2SDYN	Port2 FX differential SD input	in	-	3.3	-	-	PECL	-	-	Y11
EXTRES	Reference Resistor of 12.4 kohm	in	-	AI	-	-	-	-	-	K19
ATP	Analog Test Function	out	AO	-	-	-	-	-	-	K18
P1SDYN	Port1 FX differential SD input	in	-	3.3	-	-	PECL	-	-	A11
P1SDXP	Port1 FX differential SD input	in	-	3.3	-	-	PECL	-	-	B11
P1TDYN	Port1 FX differential transmit output	out	3.3	-	-	12	-	62,5	30	A9
P1TDXP	Port1 FX differential transmit output	out	3.3	-	-	12	-	62,5	30	B9
P1RDYN	Port1 FX differential receive input	in	-	3.3	-	-	PECL	-	-	A12
P1RDXP	Port1 FX differential receive input	in	-	3.3	-	-	PECL	-	-	B12
P1TXP	Port1 differential transmit output	bi	AO	AI	-	18	-	62,5	n/a ¹⁾	J19
P1TXN	Port1 differential transmit output	bi	AO	AI	-	18	-	62,5	n/a ¹⁾	J20
P1RXP	Port1 differential receive input	bi	AO	AI	-	18	-	62,5	n/a ¹⁾	H19
P1RXN	Port1 differential receive input	bi	AO	AI	-	18	-	62,5	n/a ¹⁾	H20
P1FXEN ²⁾	Port1 (100BASE-FX mode enabled)	out	3.3	-	-	12	-	0	30	C9
P2FXEN ²⁾	Port2 (100BASE-FX mode enabled)	out	3.3	-	-	12	-	0	30	Y8
TESTDOUT5 ²⁾	TestOut	out	3.3	-	-	12	-	0	30	B8
TESTDOUT6 ²⁾	TestOut	out	3.3	-	-	12	-	0	30	A8
TESTDOUT7 ²⁾	TestOut	out	3.3	-	-	12	-	0	30	V10

¹⁾ External circuitry defined by Renesas which is not pure capacitive. See Chapter 6.2.4

²⁾ see Table 2 how to use this pin

Hints for board-design:

See Chapter 6.2.3

2.1.4 Signalgroup "JTAG-Ports"

Signal	Signaldescription	Dir	Output (V)	Input (V)	Pull	Current (mA)	I-Typ	fout (MHz)	CL/ MAX (pF)	pinid
XTRST	JTAG – Reset	in	-	3.3	-	-	S	-	-	P4
RTCK	JTAG - Sync TCK	out	3.3	-	-	6	-	50	50	W7
TCK	JTAG – Clock	in	-	3.3	dn	-	S	-	-	P3
TDI	JTAG – Data In	in	-	3.3	-	-	S	-	--	W8
TDO	JTAG – Data Out	out ¹⁾	3.3	-	-	6	-	50	50	R7
TMS	JTAG – Test Mode Select	in	-	3.3	-	-	S	-	-	T8

XSRST	System-Reset for Debugging	bi	3.3	3.3	up	6	S	0.1	50	R10
TAP_SEL ¹⁾	TAP-Selector	in	-	3.3	-	-	S	-	-	T7
NC ¹⁾	Not used. Must be connected with a Pullup to 3,3 V	in	-	3,3	-	-	S	-	-	P6

¹⁾ see Table 2 how to use this pin

In the following table the different suggestions for the external pull wiring of the JTAG-Interface is shown.

JTAG Signal	Signal Direction	ERTEC 200P internal pull	Default circuit for the final product	Circuit for Debugging, ARM recommended	recommended JTAG circuit	Recommendation from Debug supplier (Lauterbach)
XTRST	in	-	10k pulldown	4k7 Pullup	10k Pulldown default and 4k7 Pullup Assembly option	A pull-down resistor (1k - 47k) should be placed on this signal on target side, although this is not JTAG conform. It ensures the on-chip debug logic is inactive when the debugger is not connected.
RTCK	in/out	-	<i>not necessary</i>	4k7 Pulldown	4k7 Pulldown	If this is not required, then it can be used to compensate the propagation delays on driver and cable. This allows to reach higher JTAG clock frequencies. Therefore you need to feed-back the TCK signal buffered or unbuffered to this line. On an unbuffered feed-back it might have negative effect on signal reflection. Better provide a chance to cut the connection on the target (jumper or solder bridge) in case problems arise.
TCK	In	Pulldown	<i>not necessary</i>	4k7 Pulldown	4k7 Pulldown	A pull-up or pull-down resistor (1k - 47k) should be placed on this line in order to give it a defined state even when the line is not driven by the debugger.
TDI	In	-	<i>not necessary</i>	4k7 Pullup	4k7 Pullup	A pull-up or pull-down resistor (1k - 47k) can be placed on this line to ensure a defined state even when the line is not driven by the debugger.
TMS	In	-	<i>not necessary</i>	4k7 Pullup	4k7 Pullup	A pull-up or pull-down resistor (1k - 47k) can be placed on this line in order to give it a defined state even when the line is not driven by the debugger.
XSRST	In	Pullup	<i>not necessary because of internal pullup</i>	<i>not necessary, because of internal Pullup</i>	<i>not necessary, because of internal Pullup</i>	There might be the need to place a pull-up (1k - 47k) on target side to avoid unintentional resets when the debugger is not connected and probably to strengthen the weak 47k pull-up in the debug cable.
TDO	out	-	<i>not necessary</i>	<i>not necessary</i>	330hm serial resistor	A 33 series resistor can be placed close to the processor for series termination. A pull-up or pull-down resistor (1k - 47k) can be placed on this line.

Table 1: External Pull wiring for the JTAG-Interface

Hint for board-layout:

In order to achieve the best possible noise immunity (see col. "Circuit of production" in table above), the Pin XTRST has to be tied to zero with an 10 kOhm Pulldown. This causes the deactivation of the JTAG-Interface whereby interfering impulses on the JTAG-Signals has no effects to the ERTEC 200P function. For use of a debugger on the JTAG-Interface the Pulldown has no effect, because the Debugger drives the Signal XTRST active to '1'.

2.1.5 Signalgroup “EMC”

Signal	Signaldescription	Dir	Output (V)	Input (V)	Internal Pull	Current (mA)	I-Typ	fout (MHz)	CL/ MAX (pF)	pinid
DTXR	EMC Direction signal for external driver	bi	1.8	1.8	dn	12	-	42 ¹⁾	42 ¹⁾	U6
XOE_DRIVER	EMC Enable signal for external driver	bi	1.8	1.8	up	12	-	1	42 ¹⁾	T6
A0	EMC Address-Bit 0	out	1.8	-	-	12	-	42 ¹⁾	42 ¹⁾	H4
A1	EMC Address-Bit 1	out	1.8	-	-	12	-	42 ¹⁾	42 ¹⁾	G4
A2	EMC Address-Bit 2	out	1.8	-	-	12	-	42 ¹⁾	42 ¹⁾	F4
A3	EMC Address-Bit 3	out	1.8	-	-	12	-	42 ¹⁾	42 ¹⁾	F5
A4	EMC Address-Bit 4	out	1.8	-	-	12	-	42 ¹⁾	42 ¹⁾	E4
A5	EMC Address-Bit 5	out	1.8	-	-	12	-	42 ¹⁾	42 ¹⁾	E3
A6	EMC Address-Bit 6	out	1.8	-	-	12	-	42 ¹⁾	42 ¹⁾	G1
A7	EMC Address-Bit 7	out	1.8	-	-	12	-	42 ¹⁾	42 ¹⁾	G2
A8	EMC Address-Bit 8	out	1.8	-	-	12	-	42 ¹⁾	42 ¹⁾	F3
A9	EMC Address-Bit 9	out	1.8	-	-	12	-	42 ¹⁾	42 ¹⁾	H1
A10	EMC Address-Bit 10	out	1.8	-	-	12	-	42 ¹⁾	42 ¹⁾	H2
A11	EMC Address-Bit 11	out	1.8	-	-	12	-	42 ¹⁾	42 ¹⁾	J2
A12	EMC Address-Bit 12	out	1.8	-	-	12	-	42 ¹⁾	42 ¹⁾	J1
A13	EMC Address-Bit 13	out	1.8	-	-	12	-	42 ¹⁾	42 ¹⁾	K2
A14	EMC Address-Bit 14	out	1.8	-	-	12	-	42 ¹⁾	42 ¹⁾	L2
A15	EMC Address-Bit 15	bi	1.8	1.8	dn	12	C	42 ¹⁾	42 ¹⁾	M4
A16	EMC Address-Bit 16	bi	1.8	1.8	up	12	C	42 ¹⁾	42 ¹⁾	M2
A17	EMC Address-Bit 17	bi	1.8	1.8	up	12	C	42 ¹⁾	42 ¹⁾	N2
A18	EMC Address-Bit 18	bi	1.8	1.8	up	12	C	42 ¹⁾	42 ¹⁾	N4
A19	EMC Address-Bit 19	bi	1.8	1.8	dn	12	C	42 ¹⁾	42 ¹⁾	P1
A20	EMC Address-Bit 20	bi	1.8	1.8	up	12	C	42 ¹⁾	42 ¹⁾	P2
A21	EMC Address-Bit 21	bi	1.8	1.8	dn	12	C	42 ¹⁾	42 ¹⁾	P5
A22	EMC Address-Bit 22	bi	1.8	1.8	dn	12	C	42 ¹⁾	42 ¹⁾	R3
A23	EMC Address-Bit 23	bi	1.8	1.8	up	12	C	42 ¹⁾	42 ¹⁾	R4
D0	EMC Data-Bit 0	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	Y4
D1	EMC Data-Bit 1	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	V4
D2	EMC Data-Bit 2	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	V5
D3	EMC Data-Bit 3	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	W4
D4	EMC Data-Bit 4	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	V6
D5	EMC Data-Bit 5	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	U4
D6	EMC Data-Bit 6	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	U3
D7	EMC Data-Bit 7	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	U5
D8	EMC Data-Bit 8	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	U2
D9	EMC Data-Bit 9	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	V2
D10	EMC Data-Bit 10	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	U1
D11	EMC Data-Bit 11	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	W2
D12	EMC Data-Bit 12	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	V1
D13	EMC Data-Bit 13	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	W3
D14	EMC Data-Bit 14	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	V3
D15	EMC Data-Bit 15	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	Y3
D16	EMC Data-Bit 16	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	D4

Signal	Signaldescription	Dir	Output (V)	Input (V)	Internal Pull	Current (mA)	I-Typ	fout (MHz)	CL/ MAX (pF)	pinid
D17	EMC Data-Bit 17	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	C4
D18	EMC Data-Bit 18	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	D5
D19	EMC Data-Bit 19	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	B5
D20	EMC Data-Bit 20	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	C5
D21	EMC Data-Bit 21	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	A5
D22	EMC Data-Bit 22	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	B4
D23	EMC Data-Bit 23	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	A4
D24	EMC Data-Bit 24	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	A3
D25	EMC Data-Bit 25	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	B3
D26	EMC Data-Bit 26	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	B2
D27	EMC Data-Bit 27	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	C2
D28	EMC Data-Bit 28	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	C1
D29	EMC Data-Bit 29	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	D1
D30	EMC Data-Bit 30	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	C3
D31	EMC Data-Bit 31	bi	1.8	1.8	up	12	C	62.5 ¹⁾	42 ¹⁾	D2
XWR	EMC Write Strobe	out	1.8	-	-	12	-	42 ¹⁾	42 ¹⁾	N1
XRD	EMC Read Strobe	out	1.8	-	-	12	-	42 ¹⁾	42 ¹⁾	M1
XCS_PER0	EMC Chip Select Bank 1 (ROM)Bootarea	out	1.8	-	-	12	-	1 ¹⁾	42 ¹⁾	T4
XCS_PER1	EMC Chip Select Bank 2	out	1.8	-	-	12	-	1 ¹⁾	42 ¹⁾	R5
XCS_PER2	EMC Chip Select Bank 3	out	1.8	-	-	12	-	1 ¹⁾	42 ¹⁾	D6
XCS_PER3	EMC Chip Select Bank 4	out	1.8	-	-	12	-	1 ¹⁾	42 ¹⁾	E6
XBE0_DQM0	EMC Byte Enable 0 für D(7:0)	out	1.8	-	-	12	-	42 ¹⁾	42 ¹⁾	T5
XBE1_DQM1	EMC Byte Enable 1 für D(15:8)	out	1.8	-	-	12	-	42 ¹⁾	42 ¹⁾	T3
XBE2_DQM2	EMC Byte Enable 2 für D(23:16)	out	1.8	-	-	12	-	42 ¹⁾	42 ¹⁾	E5
XBE3_DQM3	EMC Byte Enable 3 für D(31:24)	out	1.8	-	-	12	-	42 ¹⁾	42 ¹⁾	D3
XRDY_PER	EMC Ready Signal	in	-	1.8	up	-	C	-	-	G6
CLK_O_SDRAM0	EMC SDRAM Clock Out	bi	1.8	1.8	-	12	C	125 ¹⁾	42 ¹⁾	H5
CLK_O_SDRAM1	EMC SDRAM Clock Out	bi	1.8	1.8	-	12	C	125 ¹⁾	42 ¹⁾	J5
CLK_O_SDRAM2 ²⁾	EMC SDRAM Clock Out	bi	1.8	1.8	-	12	C	125 ¹⁾	42 ¹⁾	J6
CLK_I_SDRAM	EMC SDRAM Clock In	in	-	1.8	-	-	C	-	-	G5
XCS_SDRAM	EMC SDRAM chip_select low_active	out	1.8	-	-	12	-	5 ¹⁾	42 ¹⁾	J3
XRAS_SDRAM	EMC SDRAM ras low_active	out	1.8	-	-	12	-	5 ¹⁾	42 ¹⁾	J4
XCAS_SDRAM	EMC SDRAM cas low_active	out	1.8	-	-	12	-	5 ¹⁾	42 ¹⁾	K3
XWE_SDRAM	EMC SDRAM write_enable low_active	out	1.8	-	-	12	-	5 ¹⁾	42 ¹⁾	K4
XAV_BF	Address Valid Burst Flash	out	1.8	-	-	12	-	5 ¹⁾	42 ¹⁾	K5
XRDY_BF	Ready Signal Burst Flash	in	-	1.8	up	-	C			L4
CLK_O_BF0 ²⁾	EMC Burst Flash CLK Out	bi	1.8	1.8	-	12	C	125 ¹⁾	42 ¹⁾	M5
CLK_O_BF1 ²⁾	EMC Burst Flash CLK Out	bi	1.8	1.8	-	12	C	125 ¹⁾	42 ¹⁾	N5
CLK_O_BF2 ²⁾	EMC Burst Flash CLK Out	bi	1.8	1.8	-	12	C	125 ¹⁾	42 ¹⁾	M6
CLK_I_BF ²⁾	EMC Burst Flash CLK In	in	-	1.8	-	-	C	-	-	L5

¹⁾ see Chapter 6.2.1 for proper Board-Layout

²⁾ see Table 2 how to use the pin

2.1.6 Signalgroup "GPIO-Ports"

Signal	Signaldescription	Dir	Output (V)	Input (V)	Internal Pull	Current (mA)	I- Typ	fout (MHz)	CL/ MAX (pF)	pinid
GPIO0_INT	GPIO (interrupt capable)	bi	3.3	3.3	disabled	6	S	25	25	V9
GPIO1_INT	GPIO (interrupt capable)	bi	3.3	3.3	disabled	6	S	25	25	U7
GPIO2_INT	GPIO (interrupt capable)	bi	3.3	3.3	disabled	6	S	25	25	U8
GPIO3_INT	GPIO (interrupt capable)	bi	3.3	3.3	disabled	6	S	25	25	U9
GPIO4_INT	GPIO (interrupt capable)	bi	3.3	3.3	disabled	6	S	25	25	U10
GPIO5_INT	GPIO (interrupt capable)	bi	3.3	3.3	disabled	6	S	25	25	U11
GPIO6_INT	GPIO (interrupt capable)	bi	3.3	3.3	disabled	6	S	25	25	U12
GPIO7_INT	GPIO (interrupt capable)	bi	3.3	3.3	disabled	6	S	25	25	U13
GPIO8_INT	GPIO (interrupt capable)	bi	3.3	3.3	disabled	6	S	25	25	R16
GPIO9_INT	GPIO (interrupt capable)	bi	3.3	3.3	disabled	6	S	25	25	R17
GPIO10_INT	GPIO (interrupt capable)	bi	3.3	3.3	disabled	6	S	25	25	T16
GPIO11_INT	GPIO (interrupt capable)	bi	3.3	3.3	disabled	6	S	25	25	T17
GPIO12_INT	GPIO (interrupt capable)	bi	3.3	3.3	dn	6	S	25	25	T18
GPIO13_INT	GPIO (interrupt capable)	bi	3.3	3.3	dn	6	S	25	25	U17
GPIO14_INT	GPIO (interrupt capable)	bi	3.3	3.3	up	6	S	25	25	U18
GPIO15_INT	GPIO (interrupt capable)	bi	3.3	3.3	up	6	S	25	25	V17
GPIO16	GPIO	bi	3.3	3.3	dn	6	S	25	20	T9
GPIO17	GPIO	bi	3.3	3.3	dn	6	S	25	20	T10
GPIO18	GPIO	bi	3.3	3.3	disabled	6	S	25	20	T14
GPIO19	GPIO	bi	3.3	3.3	disabled	6	S	25	20	T15
GPIO20	GPIO	bi	3.3	3.3	dn	6	S	25	20	U14
GPIO21	GPIO	bi	3.3	3.3	up	6	S	25	20	U15
GPIO22	GPIO	bi	3.3	3.3	up	6	S	25	20	R18
GPIO23	GPIO	bi	3.3	3.3	dn	6	S	25	20	U16
GPIO24	GPIO	bi	3.3	3.3	dn	6	S	25	20	W19
GPIO25	GPIO	bi	3.3	3.3	dn	6	S	25	20	W18
GPIO26	GPIO	bi	3.3	3.3	up	6	S	25	20	W17
GPIO27	GPIO	bi	3.3	3.3	up	6	S	25	20	V20
GPIO28	GPIO	bi	3.3	3.3	dn	6	S	25	20	Y18
GPIO29	GPIO	bi	3.3	3.3	dn	6	S	25	20	Y17
GPIO30	GPIO	bi	3.3	3.3	dn	6	S	25	20	V19
GPIO31	GPIO	bi	3.3	3.3	dn	6	S	25	20	V18

¹⁾ The pull-direction depends on the used Configuration. See Chapter 7.6

Hint: 64 additional GPIO's are multiplexed with the XHIF-Interface.

2.1.7 Signalgroup "Host Interface"

Hint: This table shows the configuration of GPIO95 to 32 used as XHIF

Signal	Signaldescription	Dir	Output (V)	Input (V)	Internal Pull ¹⁾	Current (mA)	I- Typ	fout (MHz)	CL/ MAX (pF)	pinid
XHIF_A1	XHIF Address-Bit 1	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	A16
XHIF_A2	XHIF Address-Bit 2	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	C15
XHIF_A3	XHIF Address-Bit 3	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	B16
XHIF_A4	XHIF Address-Bit 4	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	E15
XHIF_A5	XHIF Address-Bit 5	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	D15

Signal	Signal Description	Dir	Output (V)	Input (V)	Internal Pull ¹⁾	Current (mA)	I- Typ	f _{out} (MHz)	CL/ MAX (pF)	pinid
XHIF_A6	XHIF Address-Bit 6	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	C17
XHIF_A7	XHIF Address-Bit 7	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	E16
XHIF_A8	XHIF Address-Bit 8	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	B14
XHIF_A9	XHIF Address-Bit 9	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	E17
XHIF_A10	XHIF Address-Bit 10	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	B19
XHIF_A11	XHIF Address-Bit 11	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	C18
XHIF_A12	XHIF Address-Bit 12	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	C19
XHIF_A13	XHIF Address-Bit 13	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	B15
XHIF_A14	XHIF Address-Bit 14	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	C13
XHIF_A15	XHIF Address-Bit 15	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	D17
XHIF_A16	XHIF Address-Bit 16	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	C16
XHIF_A17	XHIF Address-Bit 17	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	A15
XHIF_A18	XHIF Address-Bit 18	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	B18
XHIF_A19	XHIF Address-Bit 19	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	D19
XHIF_SEG_2	XHIF Segment-Bit 2	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	D16
XHIF_SEG_0	XHIF Segment-Bit 0	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	E18
XHIF_SEG_1	XHIF Segment-Bit 1	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	D18
XHIF_XRDY	XHIF Ready Signal	bi	1.8/3.3	1.8/3.3	- ³⁾	4 ²⁾ /9	S	25	20	L15
XHIF_XIRQ	XHIF Interrupt	bi	1.8/3.3	1.8/3.3	- ³⁾	4 ²⁾ /9	S	25	20	G15
XHIF_XWR	XHIF Write Strobe	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	D20
XHIF_XRD	XHIF Read Strobe	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	C20
XHIF_XCS_R_A20	XHIF Chip Select Register (Config) /A20	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	B17
XHIF_XCS_M	XHIF Chip Select Memory	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	A17
XHIF_XBE0	XHIF Byte Enable 0 of D(7:0)	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	F16
XHIF_XBE1	XHIF Byte Enable 1 of D(15:8)	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	F17
XHIF_XBE2	XHIF Byte Enable 2 of D(23:16)	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	E14
XHIF_XBE3	XHIF Byte Enable 3 of D(31:24)	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	F14
XHIF_D0	XHIF Data-Bit 0	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	G17
XHIF_D1	XHIF Data-Bit 1	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	L17
XHIF_D2	XHIF Data-Bit 2	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	P17
XHIF_D3	XHIF Data-Bit 3	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	G16
XHIF_D4	XHIF Data-Bit 4	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	H17
XHIF_D5	XHIF Data-Bit 5	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	L16
XHIF_D6	XHIF Data-Bit 6	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	M16
XHIF_D7	XHIF Data-Bit 7	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	K16
XHIF_D8	XHIF Data-Bit 8	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	K17
XHIF_D9	XHIF Data-Bit 9	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	M17
XHIF_D10	XHIF Data-Bit 10	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	N17
XHIF_D11	XHIF Data-Bit 11	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	J16
XHIF_D12	XHIF Data-Bit 12	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	H16
XHIF_D13	XHIF Data-Bit 13	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	N16
XHIF_D14	XHIF Data-Bit 14	bi	1.8/3.3	1.8/3.3	up	4 ²⁾ /9	S	25	20	J17
XHIF_D15	XHIF Data-Bit 15	bi	1.8/3.3	1.8/3.3	up	6/12	-			P16

Signal	Signaldescription	Dir	Output (V)	Input (V)	Internal Pull ¹⁾	Current (mA)	I-Typ	fout (MHz)	CL/MAX (pF)	pinid
XHIF_D16	XHIF Data-Bit 16	bi	1.8/3.3	1.8/3.3	up	6/12	-			E8
XHIF_D17	XHIF Data-Bit 17	bi	1.8/3.3	1.8/3.3	up	6/12	-			F7
XHIF_D18	XHIF Data-Bit 18	bi	1.8/3.3	1.8/3.3	up	6/12	-			E9
XHIF_D19	XHIF Data-Bit 19	bi	1.8/3.3	1.8/3.3	up	6/12	-			D7
XHIF_D20	XHIF Data-Bit 20	bi	1.8/3.3	1.8/3.3	up	6/12	-			D8
XHIF_D21	XHIF Data-Bit 21	bi	1.8/3.3	1.8/3.3	up	6/12	-			E12
XHIF_D22	XHIF Data-Bit 22	bi	1.8/3.3	1.8/3.3	up	6/12	-			D11
XHIF_D23	XHIF Data-Bit 23	bi	1.8/3.3	1.8/3.3	up	6/12	-			D9
XHIF_D24	XHIF Data-Bit 24	bi	1.8/3.3	1.8/3.3	up	6/12	-			D10
XHIF_D25	XHIF Data-Bit 25	bi	1.8/3.3	1.8/3.3	up	6/12	-			E7
XHIF_D26	XHIF Data-Bit 26	bi	1.8/3.3	1.8/3.3	up	6/12	-			D13
XHIF_D27	XHIF Data-Bit 27	bi	1.8/3.3	1.8/3.3	up	6/12	-			E10
XHIF_D28	XHIF Data-Bit 28	bi	1.8/3.3	1.8/3.3	up	6/12	-			D14
XHIF_D29	XHIF Data-Bit 29	bi	1.8/3.3	1.8/3.3	up	6/12	-			D12
XHIF_D30	XHIF Data-Bit 30	bi	1.8/3.3	1.8/3.3	up	6/12	-			E11
XHIF_D31	XHIF Data-Bit 31	bi	1.8/3.3	1.8/3.3	up	6/12	-			E13

¹⁾ Pull is not active because Port is configured as Output

²⁾ When operating with 1.8 V the default-Value of the Registers DRIVE47_32GPIO, DRIVE63_48GPIO, DRIVE79_64GPIO and DRIVE95_80GPIO has to be changed from 4mA to 9mA

³⁾ Pull is not active because Port is configured as Output

2.2 Power / GND Pins

Pin	Ball No.	Voltage	Description
VDD_EMC	A1, E1, K1, T1, Y1, Y5, A6, E2, T2, W5, B6, H6, N6, H7, N7	1.8 V	I/O Power Supply (15 Pins) for external memory controller
VDD_XHIF	A20, A18, A14, E19, N15, H15, F13, F8, N14, H14, G13, G8	1.8 / 3.3 V	I/O Power Supply (12 Pins) for external host interface
VDD12	K7, L7, P10, P11, L14, K14, G11, G10, K8, L8, N10, N11, L13, K13, H11, H10	1.2 V	Core Power Supply (16 Pins)
VDD15	P19, G19, N3, V7, V11, V13, C14, C10, C6	1.5 V	PHY Power Supply (9 Pins)
VDD33	Y7, Y16, Y20, W13, T19, G3, M3, F18, C12, C8, K6, R8, R13, P15, F11, P8, P13	3.3 V	I/O Power Supply (17 Pins)
GND	B1, F1, L1, R1, W1, A2, Y2, Y6, Y10, Y13, Y15, Y19, W20, T20, E20, B20, A19, A13, A10, A7, F2, R2, W6, B7, H3, L3, V8, V12, V16, P18, L18, C11, C7, F6, L6, R6, R11, R15, K15, F15, F10, G7, J7, M7, P7, P9, P12, P14, M14, J14, G14, G12, G9, H8, J8, M8, N8, N9, N12, N13, M13, J13, H13, H12, H9, J9, K9, L9, M9, M10, M11, M12, L12, K12, J12, J11, J10, K10, L10, L11, K11, B13	GND	ERTEC 200P-Ground (80 Pins)
PVSSA	N18, M18, J18, H18	GND	Analog PHY GND, can be shared with VSSAPLLCB. Recommendation: PVSSA should be separated from digital ground by filter or connected to digital ground at far end from ERTEC 200P.

Pin	Ball No.	Voltage	Description
VDDQ(PECL)x	B10, W10	3.3 V	3.3 V Supply for FX-Interface. can be shared with VDD33 Recommendation: Should be separated from analog 3.3 V VDD by filter.
VDD33ESD	G18	3.3 V	Analog Test 3.3 V Supply. Recommendation: Should be separated from ERTEC 200P I/O 3.3 V VDD by filter.
VDDACB	L20	3.3 V	Analog Central 3.3 V Supply. Recommendation: Should be separated from ERTEC 200P I/O 3.3 V VDD by filter.
PxVDDARXTX	G20, P20	1.5 V	Analog Port Tx/RX Supply, can be shared with VDDAPLL. Recommendation: Should be separated from digital 1.5 V VDD by filter.
VDDAPLL	K20	1.5 V	Analog Central 1.5 V Supply, can be shared with PxVDDARXTX. Recommendation: Should be separated from digital 1.5 V VDD by filter.
VSSAPLLCB	L19	GND	Analog Central GND. Recommendation: VSSAPLLCB should be separated from digital ground by filter or connected to digital ground at far end from ERTEC 200P.
DVDDy	F20, R20	1.5 V	Digital PHY 1.5-V VDD, can be connected to VDD15
DGNDy	F19, R19	GND	Digital Ground (GND), can be connected to ERTEC 200P ground
AVDD	V15	1.2 V	PLL Analog Power Supply (requires external filtering)
AGND	V14	GND	PLL Analog Ground

Note: x = 1, 2 and y = 1, 3

2.3 Handling of Unused Pins

IN and INOUT pins, which are not pulled internally must have an external pull resistor.

Hint:

If the internal pull-up/down resistor of a GPIO is deactivated, it must be activated from software or an external pull-up/down resistor has to be used.

See Chapter 6.2.4.1 and 6.2.5.2 for Information how to handle unused PHY-Pins

Signal	Signal description	Dir	Function description	PinID/ Ball
ATP	Analog Test Function	out	Analog Test Enable to monitor or drive specific nodes in the analog circuit during analog test. For debugging purposes it is recommended to have this pin accessible for an oscilloscope on a PCB. This pin is not used in normal operation.	K18
TEST	IC-Test-Mode	in	IC Test Mode Select signal for ASIC test. For normal operation this pin must be connected by a 1k Ohm Pull down resistor to GND.	R9
TMC1	Testmode_1	in	Test Mode Control Signal for ASIC test. For normal operation this pin must be connected directly to GND.	F12
TMC2	Testmode_2	in	Test Mode Control Signal for ASIC test. For normal operation this pin must be connected directly to GND.	R14
TACT	TESTACT-TAP-RESET	in	Special Test Mode TAP Controller Used for Boundary scan test. For normal operation this pin must be connected by a 1k Ohm Pull down resistor to GND.	R12
TAP_SEL	TAP Select	in	TAP Select Used for Boundary scan test. For normal operation this pin must be connected by a 1k Ohm Pull down resistor to GND.	T7
P1FXEN	Port 1 Fiber Optic Enable	out	Port 1 Fiber Optic Enable This pin is not used and should be unconnected. The Fiber Optic transceiver should be enabled all the time by proper pull resistor.	C9
P2FXEN	Port 2 Fiber Optic Enable	out	Port 2 Fiber Optic Enable This pin is not used and should be unconnected. The Fiber Optic transceiver should be enabled all the time by proper pull resistor.	Y8
TESTDOUT5	Test Output 5	out	Test Output 5 This pin is not used and should be unconnected.	B8
TESTDOUT6	Test Output 6	out	Test Output 6 This pin is not used and should be unconnected.	A8
TESTDOUT7	Test Output 7	out	Test Output 7 This pin is not used and should be unconnected.	V10
CLK_O_SDRAM2	EMC SDRAM Clock Out	bi	Clock Output SDRAM 2 In normal operation this signal is connected to second SDRAM, upper 16 Bit (see 6.2.1). In case where just one SDRAM is implemented an external 10k Ohm Pull up resistor must be connected.	H5
CLK_O_BF0	EMC Burst Flash CLK Out	bi	Clock Output Burst Mode Flash 0 In normal operation this signal is connected to CLK_I_BF (see 6.2.1). In case where no Burst Mode Flash is implemented an external 10k Ohm Pull up resistor must be connected.	M5
CLK_O_BF1	EMC Burst Flash CLK Out	bi	Clock Output Burst Mode Flash 1 In normal operation this signal is connected to first Burst Mode Flash, lower 16 Bit (see 6.2.1). In case where no Burst Mode Flash is implemented an external 10k Ohm Pull up resistor must be connected.	N5
CLK_O_BF2	EMC Burst Flash CLK Out	bi	Clock Output Burst Mode Flash 2 In normal operation this signal is connected to	M6

Signal	Signal description	Dir	Function description	PinID/ Ball
			second Burst Mode Flash, upper 16 Bit (see 6.2.1). In case where just one Burst Mode Flash is implemented an external 10k Ohm Pull up resistor must be connected.	
CLK_I_BF	EMC Burst Flash CLK In	in	Clock Input Burst Mode Flash In normal operation this signal is connected to CLK_O_BF0 (see 6.2.1). In case where no Burst Mode Flash is implemented an external 10k Ohm Pull up resistor must be connected.	L5
NC	Reserved	in	Reserved This pin is not used and must be connected by a 1k Ohm Pull up resistor to VDD33.	P6

Table 2: Recommendation for handling special function signals

3 Maximum Ratings

Parameter	Symbol	Conditions	Min	Max	Unit
Power supply voltage	VDD12	1.2 V type	-0.5	+1.6	V
	VDD15 PxVDDARXTX VDDAPLL DVDDy	1.5 V type	-0.5	+2.0	V
	VDD33 VDDQ(PECL)x VDD33ESD VDDACB	3.3 V type	-0.5	+4.6	V
I/O voltage	VDD_EMC / VDD_XHIF	1.8 V buffer	-0.5	+2.5	V
	VDD_XHIF	3.3 V buffer	-0.5	+4.6	V
Output current (1.8V / /3.3V buffer)	I _o	2 mA type		17.1	mA
		4 mA type		34.3	mA
		6 mA type		34.3	mA
		8 mA type		34.3	mA
		12 mA type		34.3	mA
Junction temperature	T _J		-40	+125	°C
Storage temperature ¹	T _{STG}		-65	+125	°C
Storage temperature ²	T _{STG}		+5	+35	°C

Table 3: Maximum Ratings

Note: x = 1, 2 and y = 1, 3

¹ conditions for soldered asics

² conditions for storing in the 'dry-package' without need of prebaking. See chapter 9.3 for the prebaking temperature and duration.

Stresses greater than those listed in above table may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

4 AC- and DC-Characteristics

4.1 Power Dissipation

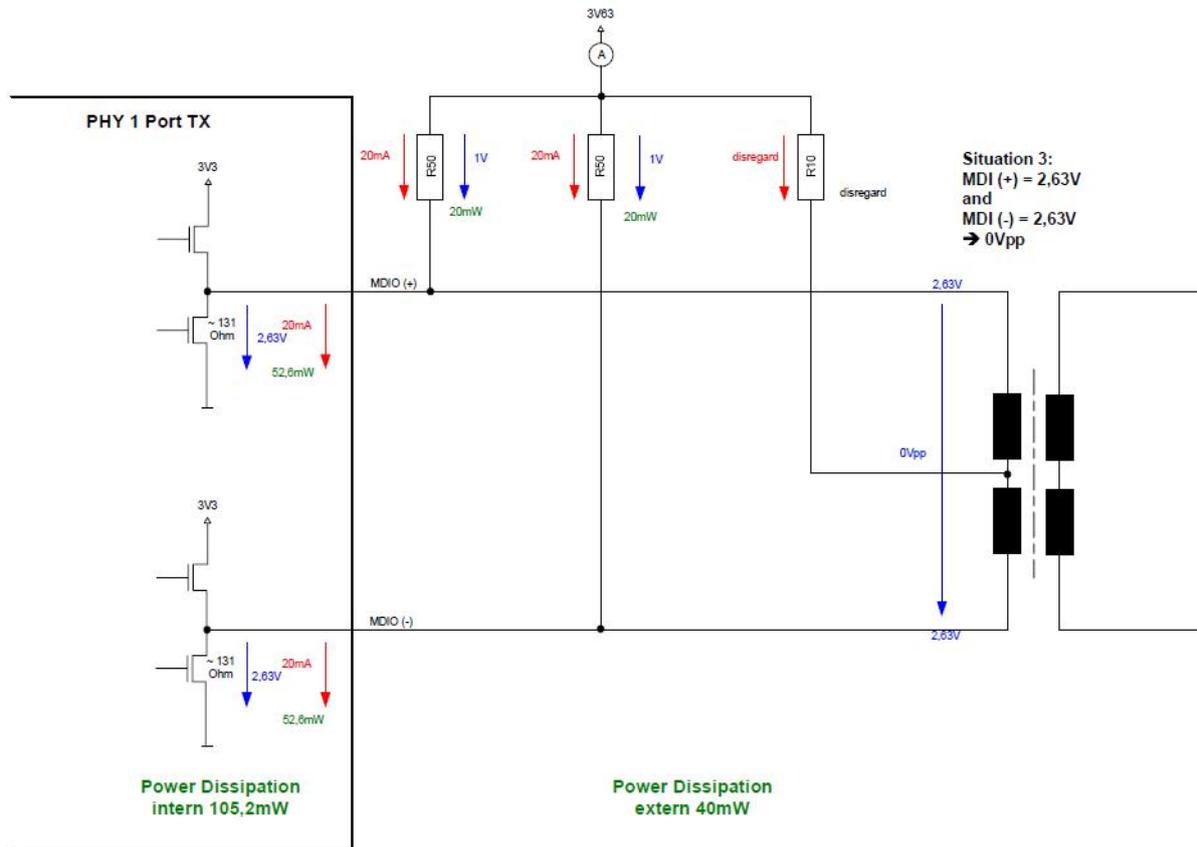
Total Power Dissipation ERTEC 200P with PHY in 100BASE-TX mode: **max. 1,52 W**
typ. 0,95 W

Total Power Dissipation ERTEC 200P with PHY in 100BASE-FX mode: **max. 1,17 W**
typ. 0,69 W

Power Dissipation ERTEC 200P	Voltage typ. (max.)	Power Dissipation		Current Consumption	
		typ.	max.	typ.	max.
Ethernet Dual PHY 100BASE-TX mode	3,3V (+ 10%) 1,5V (+ 10%)	139 mW 225 mW	210 mW*) 277 mW	80 mA 152 mA	80 mA 168 mA
IO-Pads 1,8V (EMC) IO-Pads 1,8V / 3,3V (XHIF) IO-Pads 3,3V (GPIO, ..)	1,8V (+ 10%) 1,8V / 3,3V (+ 10%) 3,3V (+ 10%)	65 mW 20mW / 66 mW 21 mW	93 mW 22mW / 73 mW 29 mW	36 mA 11mA / 20 mA 7mA	47 mA 11mA / 20 mA 8 mA
Core (ARM926, KRISC, PLL, Clock, Logic, Memories)	1,2V (+ 0,1V)	426 mW	828 mW	355 mA	628 mA
ERTEC 200P 100 BASE-TX	1,2V (+ 0,1V) 1,5V (+ 10%) 1,8V (+ 10%) 3,3V (+ 10%)	0,95 W	1,52 W 1,32 W (at VDD +5%)	363 mA 152 mA 36 mA 107 mA	637 mA 168 mA 47 mA 108 mA

*) the illustrated power dissipation (105,2mW pro port) is the part of the phy which cannot be calculated regarding the current-consumption (constant 80 mA). The reason is that the external occurring part of the power dissipation (40 mW pro port) must not included into the power dissipation of the ERTEC 200P.

Table 4: Power Dissipation TX mode



Power Dissipation ERTEC 200P	Voltage typ. (max.)	Power Dissipation		Current Consumption	
		typ.	max.	typ.	max.
Ethernet Dual PHY 100BASE-FX mode	3,3V (+ 10%) 1,5V (+ 10%)	5 mW 100 mW	6 mW 125 mW	1,5 mA 67 mA	1,7 mA 76 mA
IO-Pads 1,8V (EMC)	1,8V (+ 10%)	65 mW	93 mW	36 mA	47 mA
IO-Pads 1,8V / 3,3V (XHIF)	1,8V / 3,3V (+ 10%)	20mW / 66 mW	22mW / 73 mW	11mA / 20 mA	11mA / 20 mA
IO-Pads 3,3V (GPIO, ..)	3,3V (+ 10%)	21 mW	29 mW	7mA	8 mA
Core (ARM926, KRISC, PLL, Clock, Logic, Memories)	1,2V (+ 0,1V)	426 mW	828 mW	355 mA	628 mA
ERTEC 200P 100 BASE-FX	1,2V (+ 0,1V) 1,5V (+ 10%) 1,8V (+ 10%) 3,3V (+ 10%)	0,69 W	1,17 W	363 mA 67 mA 36 mA 29 mA	637 mA 76 mA 47 mA 30 mA

Table 5: Power Dissipation FX mode

4.2 DC Operating Conditions

Note: Positive currents are flowing into the device, negative currents are flowing out of the device.

Parameter	Symbol	Min	Typ	Max	Unit
IO power supply voltage	VDD_EMC	1,8 – 10%	1,8	1,8 + 10%	V
IO power supply voltage	VDD_XHIF				
IO power supply voltage	VDD_XHIF	3,3 – 10%	3,3	3,3 + 10 %	V
IO power supply voltage	VDD33				
3.3 V Supply for FX-Interface	VDDQ(PECL)x				
Core ERTEC 200P Die	VDD12	1,1	1,2	1,3	V
PLL Analog Power Supply	AVDD	1,1	1,2	1,3	V
Core PHY Die	VDD15	1,5 – 10 %	1,5	1,5 + 10 %	V
Digital PHY 1.5-V VDD	DVDDy				
Analog Central 1.5 V Supply	VDDAPLL	1,5 – 10 %	1,5	1,5 + 10 %	V
Analog Port Tx/Rx Supply	PxVDDARXTX				
Analog Central 3.3 V Supply	VDDACB	3,3 – 10 %	3,3	3,3 + 10 %	V
Analog Test 3.3 V Supply	VDD33ESD	3,3 – 10 %	3,3	3,3 + 10 %	V
Low level input voltage (1.8V)	V _{IL}	-0.3		V _{DD} x 0.35	V
High level input voltage (1.8V)	V _{IH}	V _{DD} x 0.65		V _{DD} + 0.3	V
Low level input voltage (3.3V)	V _{IL}	-0.3		0.8	V
High level input voltage (3.3V)	V _{IH}	2.0		V _{DD} + 0.3	V
Input rise / fall time ¹⁾	t _{RFIO}	0		200	ns
fall. trigger voltage (Schmitt, 1.8V)	V _{ifall}	0.4			V
rise trigger voltage (Schmitt, 1.8V)	V _{irise}			1.3	V
Hysteresis voltage (Schmitt, 1.8V)	V _H	0.2			V
fall. trigger voltage (Schmitt, 3.3V)	V _{ifall}	0.8			V
rise trigger voltage (Schmitt, 3.3V)	V _{irise}			2	V
Hysteresis voltage (Schmitt, 3.3V)	V _H	0.3			V
Input rise / fall time (Schmitt) ¹⁾	t _{RFS}	0		1	ms
Input current 1.8 V buffer (V _{IN} = 0V or V _I = VDD)	I _{IN}			±10	µA
Input current 3.3 V buffer (V _{IN} = 0V or V _I = VDD)	I _{IN}			±5	µA
Input current 1.8 V buffer (V _{IN} = 0V, pull-up 50k)	I _{IN}	-26		-52	µA
Input current 1.8 V buffer (V _{IN} = VDD, pull-down 50k)	I _{IN}	26		52	µA
Input current 3.3 V buffer (V _{IN} = 0V, pull-up 50k)	I _{IN}	-48		-96	µA
Input current 3.3 V buffer (V _{IN} = VDD, pull-down 50k)	I _{IN}	48		96	µA
Output high voltage (I _{OH} = 0 mA)	V _{OH}	VDD_IO -0.1			V
Output low voltage (I _{OL} = 0 mA)	V _{OL}			0.1	V
Operating ambient temperature	T _a	-40		+85	°C

Table 6: DC Operating Conditions

¹⁾ Input voltage rising from 10% to 90% or falling from 90% to 10% of its nominal value

Hint: a detailed description of the Power / GND-Pins is listed in Chapter 2.2.

The tolerance of the supply voltages includes the ripple on the supply voltage, i.e. the supply voltages including the ripples may not fall under the lower border or rise above the higher border.

5 AC-Parameter (Timing, Constraining)

5.1 EMC Interface

Note:

EXTENDED_CONFIG.SODM must be set to 1 to ensure valid timing for the SDRAM data outputs.

EXTENDED_CONFIG.BFODM must be set to 1 to ensure valid timing for Burstflash.

BF_CONFIG.BF_CLK_F must be kept at 0 to ensure valid timing for Burstflash.

5.1.1 SDRAM Interface

The combination of the control signals XCS_DRAM, XRAS_SDRAM, XCAS_SDRAM, XWE_SDRAM and XBEy_DQMy together with the Address bus is defining SDRAM commands in the following way:

SDRAM command	XCS_SDRAM	XRAS_SDRAM	XCAS_SDRAM	XWE_SDRAM	XBEy_DQMy	A	Description
COMMAND INHIBIT (NOP)	1	X	X	X	X	X	No operation
NO OPERATION (NOP)	0	1	1	1	X	X	No operation
ACTIVE	0	0	1	1	X	BA/Row	Select bank and activate row
READ	0	1	0	1	1/0	BA/Col	Select bank and column, and start READ Burst
WRITE	0	1	0	0	1/0	BA/Col	Select bank and column, and start WRITE Burst
BURST TERMINATE	0	1	1	0	X	X	Terminate Burst sequence
PRECHARGE	0	0	1	0	X	Code	Deactivate row in bank or banks
AUTO REFRESH	0	0	0	1	X	X	Enter self refresh mode
LOAD MODE REGISTER	0	0	0	0	X	Op-Code1	Setup of the device specific configuration register
LOAD EXTENDED MODE REGISTER	0	0	0	0	X	Op-Code2	Setup of the device specific extended mode configuration register (e.g. mobile SDRAM devices)

Table 7: Definition of SDRAM commands

Hint: X means don't care. y = 0, 1, 2, 3

5.1.1.1 SDRAM Timing for a read access

The Output-Signals are launched with CLK_O_SDRAMx, the Input-Signals are latched in with CLK_I_SDRAM.

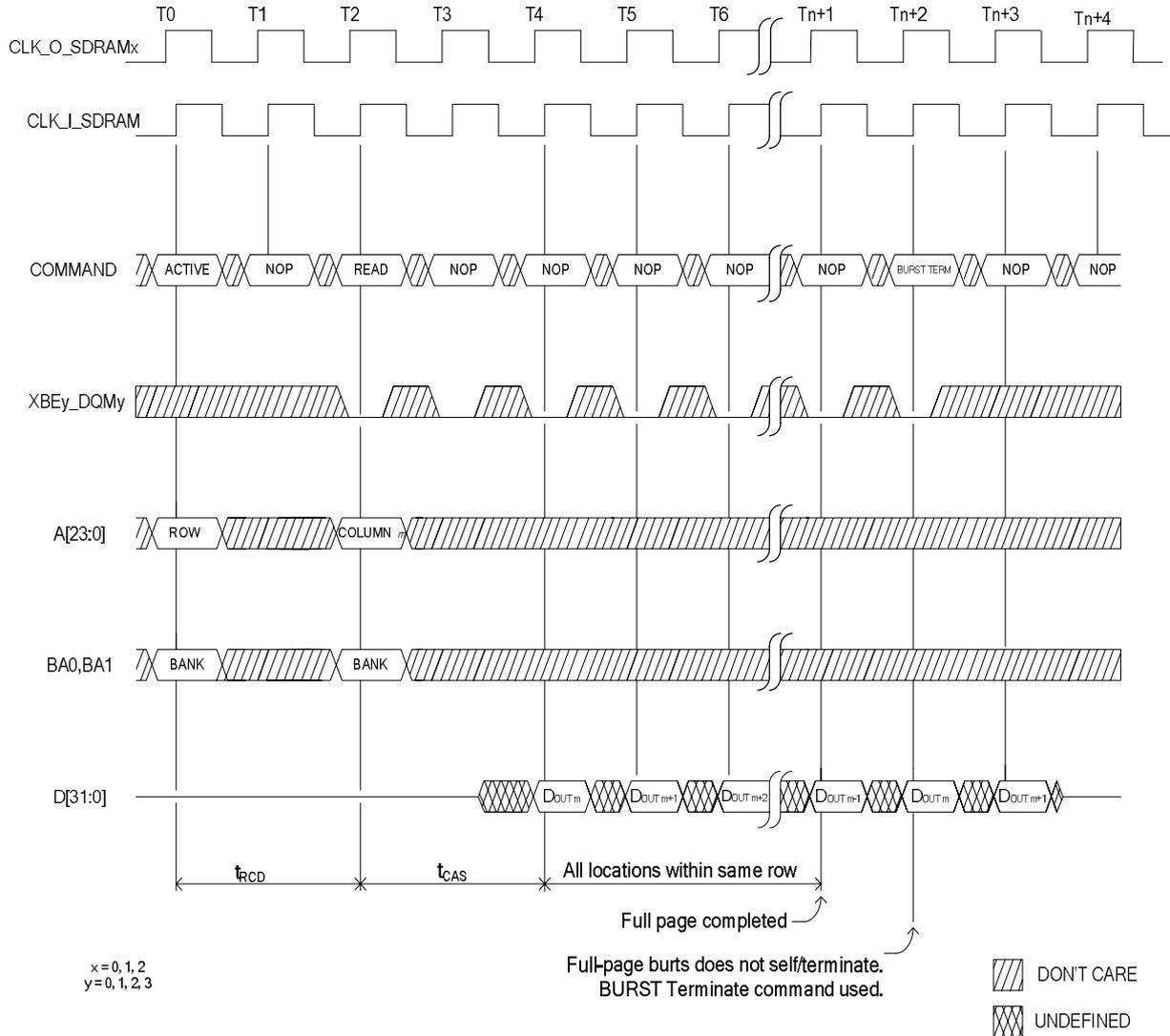


Figure 2: SDRAM – Timing for a read access

Note: The Bank signals BA0, BA1 are part of the address bus A. They are given here separately for a better understanding.

Parameter	Description	Min	Max	depends on Register
t_{RCD}	RAS to CAS delay	16 ns	32 ns	EXTENDED_CONFIG.TRCD
t_{CAS}	CAS Latency	16 ns	24 ns	SDRAM_CONFIG.CL

Table 8: Timing for a SDRAM read access

Hint:

Setup and hold times for address, command and data are the same as by a write access. They can be found in Chapter 5.1.1.2

5.1.1.2 SDRAM Timing for write access

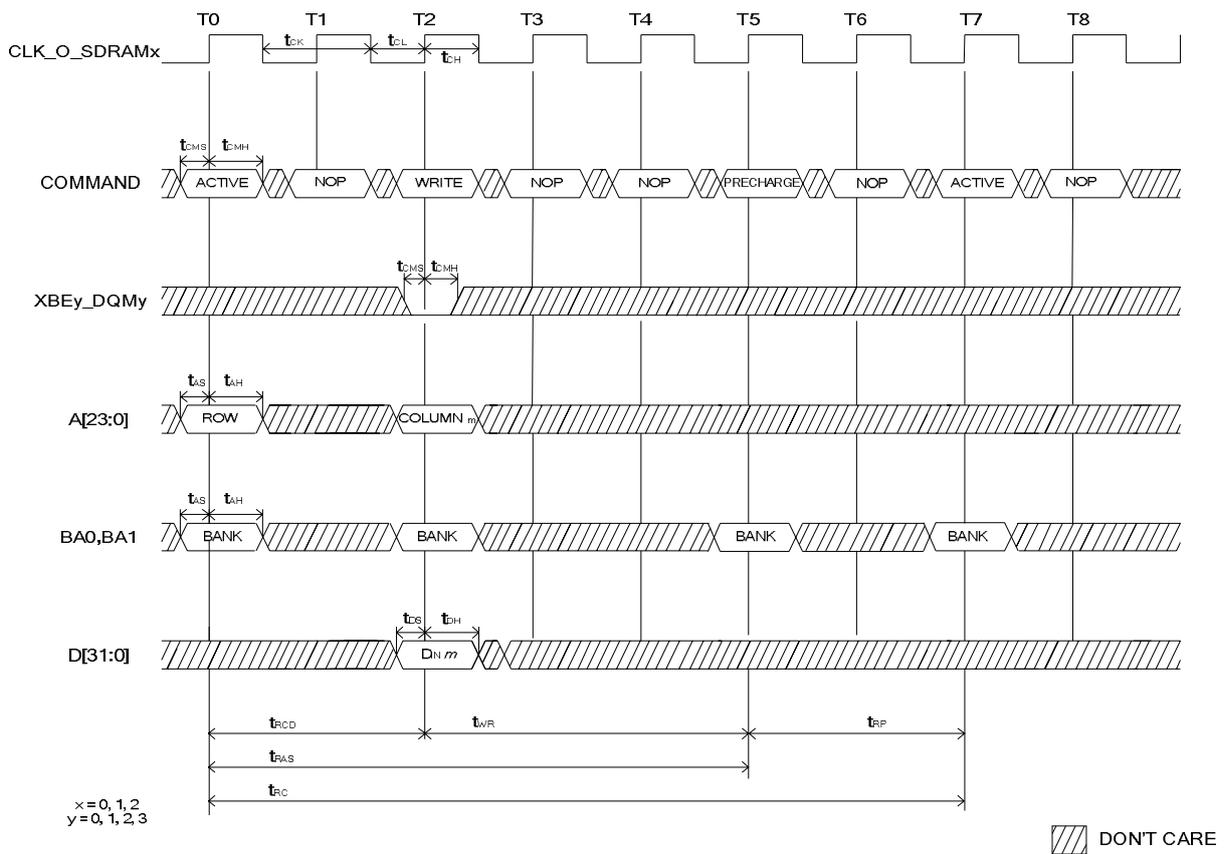


Figure 3: SDRAM – Timing for a write access

Note: The Bank signals BA0, BA1 are part of the address buss A. They are given here separately for a better understanding.

Parameter	Description	Min	Max	depends on Register
t_{CK}	Clock Period	7.8 ns	8.2 ns	-
t_{CL}	Clock Low Time	3.6 ns	4.4 ns	-
t_{CH}	Clock High Time	3.6 ns	4.4 ns	-
t_{CMS}	Command Setup Time	3.27 ns	5.87 ns	-
t_{CMH}	Command Hold Time	1.03 ns	2.39 ns	-
t_{AS}	Address Setup Time	3.70 ns	5.91 ns	-
t_{AH}	Address Hold Time	0.97 ns	2.16 ns	-
t_{DS}	Data Setup Time	3.72 ns	5.96 ns	-
t_{DH}	Data Hold Time	0.86 ns	2.02 ns	-
t_{RCD}	RAS to CAS delay	24 ns	40 ns	EXTENDED_CONFIG.TRCD
t_{RAS}	Row Address Strobe	$t_{RCD} + t_{WR}$	¹⁾	
t_{RC}	ROW cycle Time	$t_{RCD} + t_{WR} + t_{RP}$	-	-
t_{WR}	Write to Precharge Time	16 ns	¹⁾	-
t_{RP}	Row precharge latency	24 ns	24 ns	-

¹⁾ Depends on Refresh Cycle Time

Table 9: Timing for a SDRAM write access

See register description of the EMC-Module in /1/ for more information about the config-registers.

5.1.2 SRAM Interface

The use of XRDY_PER is optional and can be enabled with ASYNC_BANKx.EW. Wait-States can be inserted if XRDY_PER is used.

Hint:

For the asynchronous SRAM interface an “**active interface**” is selectable. Active interface means that at the end of a transfer the data bus is actively driven high for one AHB clock cycle. This is necessary together with the use of internal pullups to speed up the reloading of the wiring capacity.

After the active phase the internal pullups are driving the data bus and there is no need for external pullups on the board.

5.1.2.1 SRAM Timing for a read access

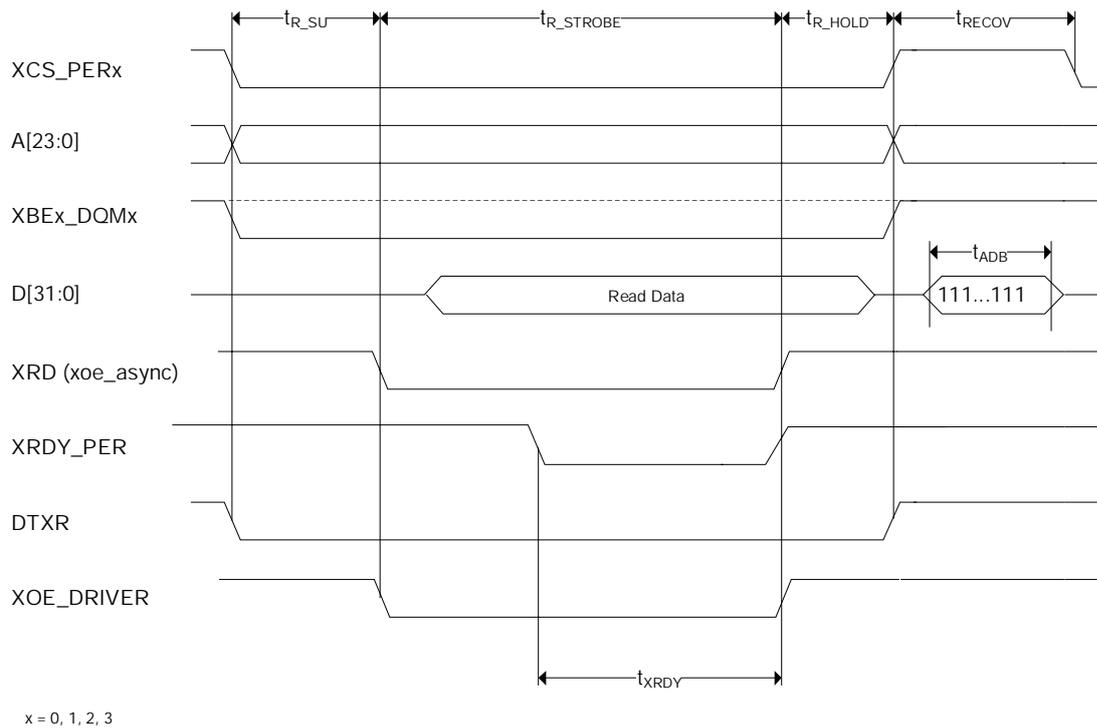


Figure 4: SRAM – Timing for a read access

Parameter	Description	Min	Max	depends on Register
t_{R_SU}	Read Setup-Time	0 ns	120 ns	ASYNC_BANKx.R_SU
t_{R_STROBE}	Read Strobe-Time	8 ns	512 ns	ASYNC_BANKx.R_STROBE
t_{R_HOLD}	Read Hold-Time	8 ns	64 ns	ASYNC_BANKx.R_HOLD
t_{XRDY}	not ready pulse width	16 ns		ASYNC_BANKx.EW
t_{ADB}	active data bus	8 ns	8 ns	EXTENDED_CONFIG.ADB
t_{RECOV}	Recovery Phase	0 ns	120 ns	RECOV_CONFIG.RECOVx

Table 10: Timing for a SRAM read access

See register description of the EMC-Module in /1/ for more information about the config-registers.

5.1.2.2 SRAM Timing for a write access

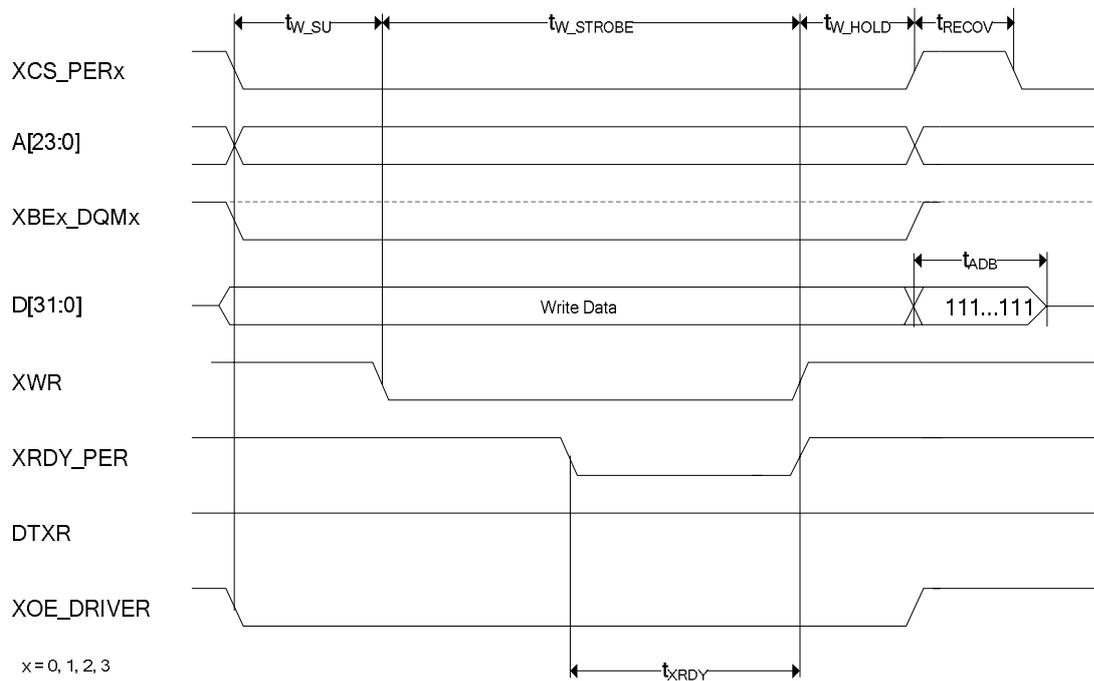


Figure 5: SRAM – Timing for a write access

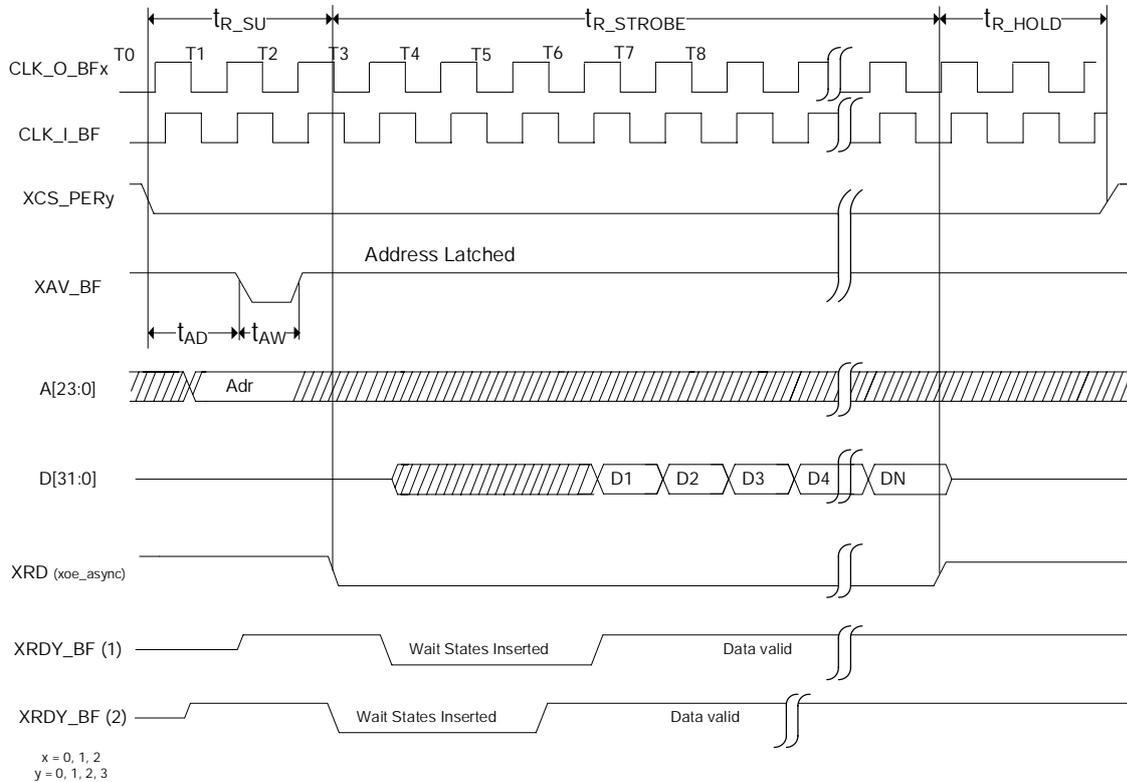
Parameter	Description	Min	Max	depends on Register
t_{W_SU}	Write Setup-Time	0 ns	120 ns	ASYNC_BANKx.W_SU
t_{W_STROBE}	Write Strobe-Time	8 ns	512 ns	ASYNC_BANKx.W_STROBE
t_{W_HOLD}	Write Hold-Time	8 ns	64 ns	ASYNC_BANKx.W_HOLD
t_{XRDY}	not ready pulse width	16 ns		ASYNC_BANKx.EW
t_{ADB}	active data bus	8 ns	8 ns	EXTENDED_CONFIG.ADB
t_{RECOV}	Recovery Phase	0 ns	120 ns	RECOV_CONFIG.RECOVx

Table 11: Timing for a SRAM write access

See register description of the EMC-Module in /1/ for more information about the config-registers.

5.1.3 BurstFlash Interface

The default-configuration for BurstFlash is asynchronous. The Timing is the same as for SRAM-Interface (see Chapter 5.1.2.1 and 5.1.2.2). For burst-Operation a setup is needed in the EMC-Controller (e.g. set BF_CONFIG.SYNC_READ to 1) and BurstModeFlash Device. The Input-Signals are latched in with CLK_I_BF.



Notes:

- (1) XRDY_BF active with BF_CONFIG.RDY_DELAY = 0
- (2) XRDY_BF active with BF_CONFIG.RDY_DELAY = 1

Figure 6: BurstFlash – Timing for a read-burst

Parameter	Description	Min	Max	depends on Register
t _{R_SU}	Read Setup-Time	0 ns	120 ns	ASYNC_BANKx.R_SU
t _{R_STROBE}	Read Strobe-Time	8 ns	512 ns	ASYNC_BANKx.R_STROBE
t _{R_HOLD}	Read Hold-Time	8 ns	64 ns	ASYNC_BANKx.R_HOLD
t _{AD}	Address Valid Delay	8 ns	128 ns	BF_CONFIG.AVD_DELAY
t _{AW}	Address Valid Pulse Width	8 ns	64 ns	BF_CONFIG.AVD_PW

Table 12: Timing for a BurstFlash read-burst

See register description of the EMC-Module in /1/ for more information about the config-registers.

5.2 Host-Interface (XHIF)

The XHIF-Part of the Hostinterface is a parallel interface. No Clock is given out. The following figure shows the timing, when the External Host initiates a Read Access.

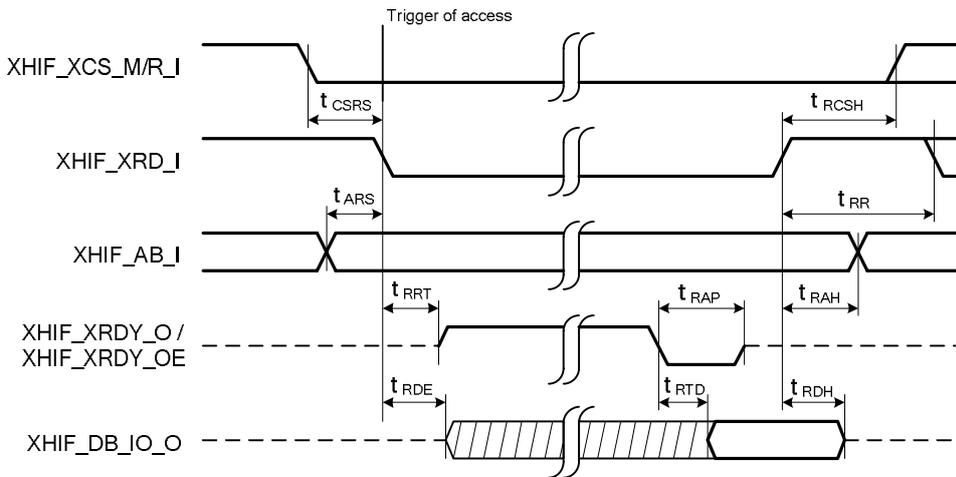


Figure 7: XHIF - Sequence for a read access

Parameter	Description	Min	Max
t_{CSRS}	chip select asserted to read pulse asserted delay	0 ns ¹⁾	
t_{ARS}	address valid to read pulse asserted setup time	0 ns	
t_{RRT}	read pulse asserted to ready deasserted delay	0 ns	10.75 ns
t_{RDE}	read pulse asserted to data enable delay	0 ns	10.75 ns
t_{RAP}	ready active pulse width	6 ns	10 ns
t_{RTD}	ready asserted to data valid delay		2.6 ns
t_{RCSH}	read pulse deasserted to chip select deasserted delay	0 ns ²⁾	
t_{RAH}	address valid to read pulse deasserted hold time	0 ns	
t_{RDH}	data valid/enable to read pulse deasserted hold time	0 ns	10.75 ns
t_{RR}	read recovery time	10.6 ns	

¹⁾ If $t_{CSRS} < 0$, t_{ARS} , t_{RRT} and t_{RDE} are related to the falling edge of XHIF_XCS

²⁾ If $t_{RCSH} < 0$, t_{RAH} and t_{RDH} are related to the rising edge of XHIF_XCS

Table 13: Timing for a XHIF read access

Write Access:

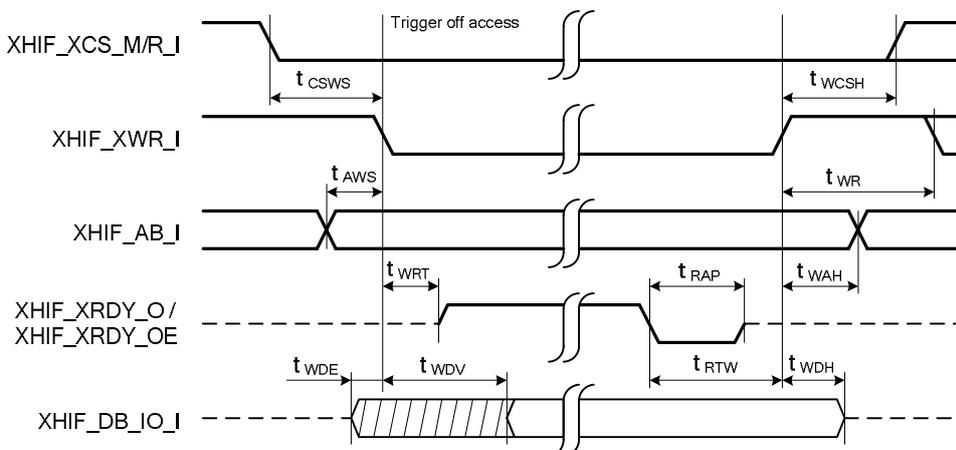


Figure 8: XHIF - Sequence for a write access

Parameter	Description	Min	Max
t_{CSWS}	chip select asserted to write pulse asserted delay	0 ns ¹⁾	
t_{AWS}	address valid to write pulse asserted setup time	0 ns	
t_{WRT}	write pulse asserted to ready deasserted delay	0 ns	10.86 ns
t_{WDE}	write pulse asserted to data enable setup	0 ns	³⁾
t_{WDV}	write pulse asserted to data valid delay		13.4 ns
t_{RAP}	ready active pulse width	6 ns	10 ns
t_{WCSH}	write pulse deasserted to chip select deasserted delay	0 ns ²⁾	
t_{WAH}	address valid to write pulse deasserted hold time	0 ns	
t_{RTW}	ready asserted to write pulse deasserted delay	0 ns	
t_{WDH}	data valid/enabled to read pulse deasserted hold time	0 ns ²⁾	
t_{WR}	write recovery time	10.6 ns	

¹⁾ If $t_{CSWS} < 0$, t_{AWS} , t_{WRT} and t_{WDE} are related to the falling edge of XHIF_XCS

²⁾ If $t_{WCSH} < 0$, t_{WAH} and t_{WDH} are related to the rising edge of XHIF_XCS

³⁾ t_{WDE} may get any value, as long as it is assured, that there is 1 idle cycle (of the XHIF clock period) guaranteed between the end of the preceding access and the start of the current access (indicated by the falling edge of XCS/XWR). Within this idle cycle no access is allowed at all.

Table 14: Timing for a XHIF write access

5.3 SPI Interfaces

A load of min. 10 pF and max 30 pF is assumed.

With a 125 MHz AHB clock the SPI baud rate ranges from 1.922 kHz to 25 MHz in master mode and a maximum of 10,42 MHz in slave mode:

$$F_{CLKOUT} = 125 \text{ MHz} / \text{SSPCPSR} * (1 + \text{SSPCR0.SCR})$$

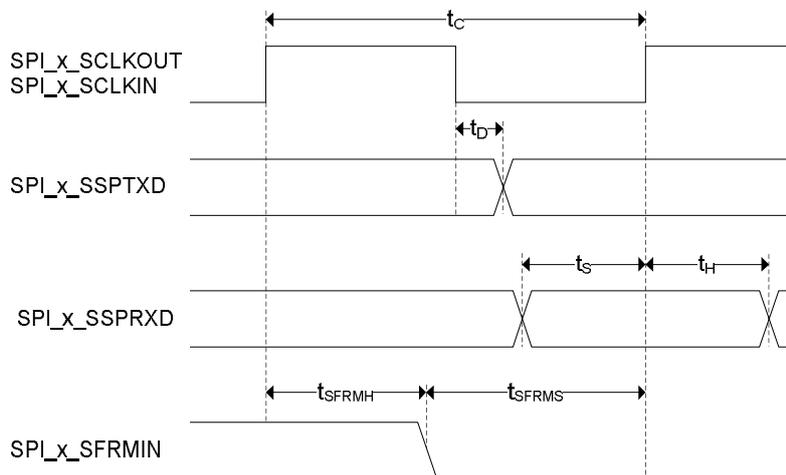
with

SPI-Master: SSPCPSR = 2..254 (even values only)

SSPCR0.SCR = 0..255

SPI-Slave: SSPCPSR = 2..254 (even values only)

SSPCR0.SCR = 2..255



x = 1, 2

Symbol	Parameter	Min.	Max.	Unit	Note
t_C	Baud rate	40 48	520000	ns	Master mode Slave mode
t_D	Valid delay	-3	3	ns	¹⁾
t_S	Setup Time	9		ns	²⁾
t_H	Hold Time	0		ns	²⁾
t_{SFRMS}	SFRMIN Setup Time	8		ns	
t_{SFRMH}	SFRMIN Hold Time	16		ns	

¹⁾ Load capacitance = 30pF

²⁾ $T_s, T_h >$ one 125 MHz period; inputs are synchronized with AHB Clock (FSSPCLK).

Table 15: Timing for a SPI access

To avoid damage caused by contention on the SPI outputs, serial resistors are recommended to reduce the maximum current.

5.4 PNPLL

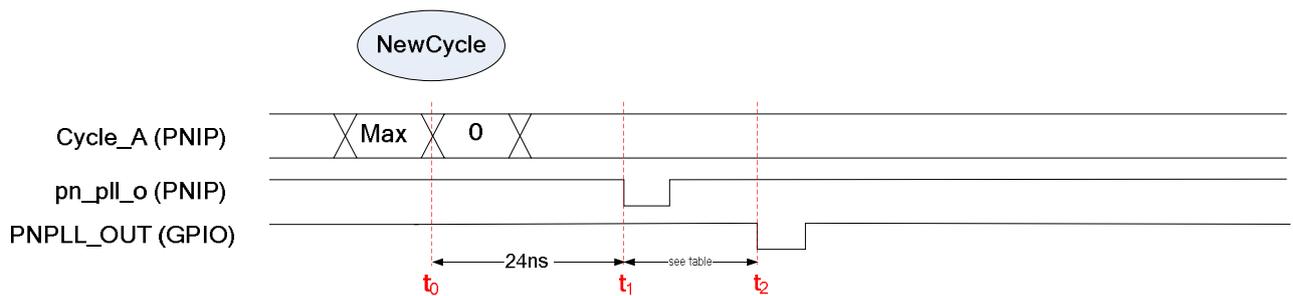
The nine output-signals PNPLL_out(8..0) can be routed to external Pins via GPIOs.

The following parameterization in the PN-IP must be done therefore:

- Register *CycleCompare_A_1* = 0x0000_0000 (Trigger-Impuls on Cycle-start)
- Register *PLL_OUT_Control_0* = 0x0000_0016 (Event appears on Signal pn_pll_o(0))

On the ERTEC 200P Toplevel the multiplexers and GPIOs must be adapted accordingly.

On the selected GPIO-Pin PNPLL_OUT can be measured. It is generated as follows:



t_0 : Cycle-start, i.e. point of time in which the Cycle-Timer breaks from a maximum value to its minimal value.

t_1 : pn_pll_o is emitted from the PNIP

t_2 : The signal PNPLL_OUT appears on the external GPIO-Pin

In the PN-IP the following delay is generated:

	Time	Description	Min/Max (ns)
PN-IP	$t_0 \rightarrow t_1$	Time from Cycle_A-break to change of the PN-IP internal Flip-Flop pn_pll_o(0) from 1 to 0.	24ns (exactly three 8ns-Clocks)
ERTEC 200P	$t_1 \rightarrow t_2$	Output_delay from one of the following PN-PLL-Outputs from PN-IP to GPIO-Pin.	see following table

Signal (Input)	Ports	Alternate Function	Input_delay			Load (pF) Min / Max
			-min	-max		
PNPLL_EXTIN_A	GPIO_9	A	1.58ns	3.00ns		-
	GPIO_23	B	1.52ns	2.77ns		-
Signal			Clock-to-Output_delay		Cycle-start to Output delay	

(Output)			(t ₁ -> t ₂)		(t ₀ -> t ₂)		
			-min	-max	-min	-max	
PNPLL_OUT0	GPIO_0	A	4,98ns	13,30ns	28,98ns	37,30ns	10 / 30
	GPIO_56	C	4,34ns	11,04ns	28,34ns	35,04ns	10 / 30
PNPLL_OUT1	GPIO_1	A	5,02ns	12,76ns	29,02ns	36,76ns	10 / 30
	GPIO_57	C	4,35ns	11,08ns	28,35ns	35,08ns	10 / 30
PNPLL_OUT2	GPIO_2	A	4,90ns	12,95ns	28,90ns	36,95ns	10 / 30
	GPIO_58	C	4,35ns	10,91ns	28,35ns	34,91ns	10 / 30
PNPLL_OUT3	GPIO_3	A	4,93ns	12,30ns	28,93ns	36,30ns	10 / 30
	GPIO_59	C	4,36ns	10,88ns	28,36ns	34,88ns	10 / 30
PNPLL_OUT4	GPIO_4	A	4,78ns	12,17ns	28,78ns	36,17ns	10 / 30
	GPIO_60	C	4,30ns	11,78ns	28,30ns	35,78ns	10 / 30
PNPLL_OUT5	GPIO_5	A	4,85ns	12,09ns	28,85ns	36,09ns	10 / 30
	GPIO_61	C	4,24ns	10,68ns	28,24ns	34,68ns	10 / 30
PNPLL_OUT6	GPIO_6	A	4,76ns	11,87ns	28,76ns	35,87ns	10 / 30
	GPIO_29	C	4,32ns	10,88ns	28,32ns	34,88ns	10 / 30
PNPLL_OUT7	GPIO_7	A	4,47ns	11,08ns	28,47ns	35,08ns	10 / 30
	GPIO_30	C	4,35ns	10,81ns	28,35ns	34,81ns	10 / 30
PNPLL_OUT8	GPIO_8	A	4,79ns	11,84ns	28,79ns	35,84ns	10 / 30
	GPIO_31	C	4,34ns	10,81ns	28,34ns	30,81ns	10 / 30

Table 16: Timing PNPLL Interface

5.5 Time-Sync Interface

The described function might not yet be supported by the PROFINET stack version delivered with the Evaluation Kit ERTEC 200P. Please refer to the User Interface Description of the Evaluation Kit for supported functionality.

Nevertheless it is recommended to layout the two signals PNPLL_EXTIN_Time and PNPLL_Time_Out according to your design to test points to contact the signals if necessary.

Signal (Input)	Ports	Alternate Function	Input_delay		Load (pF) Min / Max
			-min	-max	
PNPLL_EXTIN_Time	GPIO_12	A	1,68ns	3,34ns	-
Signal (Output)			Clock-to-Output_delay		
			-min	-max	
PNPLL_Time_Out	GPIO_11	A	4,86ns	12,09ns	10 / 30
	GPIO_28	C	4,26ns	10,73ns	10 / 30

Table 17: Timing Time-Sync Interface

5.6 JTAG-Interface

The JTAG-Interface consists of the signals TCK, TMS, TDI, TDO and TRST. All inputs besides TRST are sampled with the rising edge of TCK. The TDO signal is launched with the falling edge of TCK.

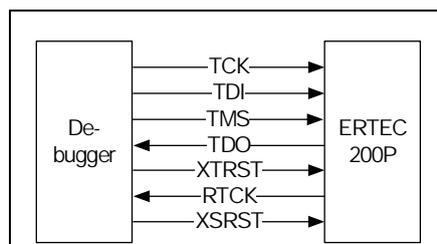


Figure 9: Debug Interface

The JTAG Clock can be used to frequency up to 32 MHz (at RTCK analysis in the debugger). For the inputs of the debug interface a minimal setup-time of 0ns should be used. Debuggers without RTCK support can use only up to 16 MHz as JTAG Clock.

5.7 Trace-Interface

The ARM926 trace is captured in an integrated Trace Buffer (ETB). The size of the buffer is 8KB (2K x 32 Bit). The Trace Buffer can be read out after a measurement over the JTAG-Interface. Both Clock-Cycles are supported (125/250 MHz).

A Debugger can be connected externally to the Trace Port. Only the ARM926 Clock-cycle of 125 MHz is supported in this case.

The Trace-Interface consists on Outputs of the ERTEC 200P and is constrained relative to the Trace-Clock. The Trace-Clock has a maximum frequency of 62,5 MHz. The data is launched with the rising and the falling edge of the Clock. A Setup-Time of 2ns and a Hold-Time of 1ns is recommended.

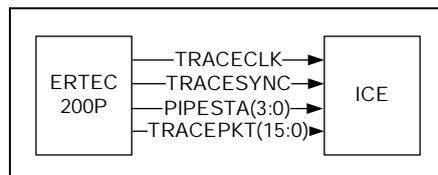


Figure 10: ARM926 Trace Interface

The Trace-Interface corresponds to the conditions given in the ETM9 specification (see /2/). If one assumes that a tracing of the ERTEC 200P is not carried out under the maximum conditions, in the constraining is enough security. (For comparison only: The Current Debugger needs a setup-time of 0,3ns and a hold-time of 0,3ns relative to the trace-clock).

6 Design Considerations

6.1 Power Sequence

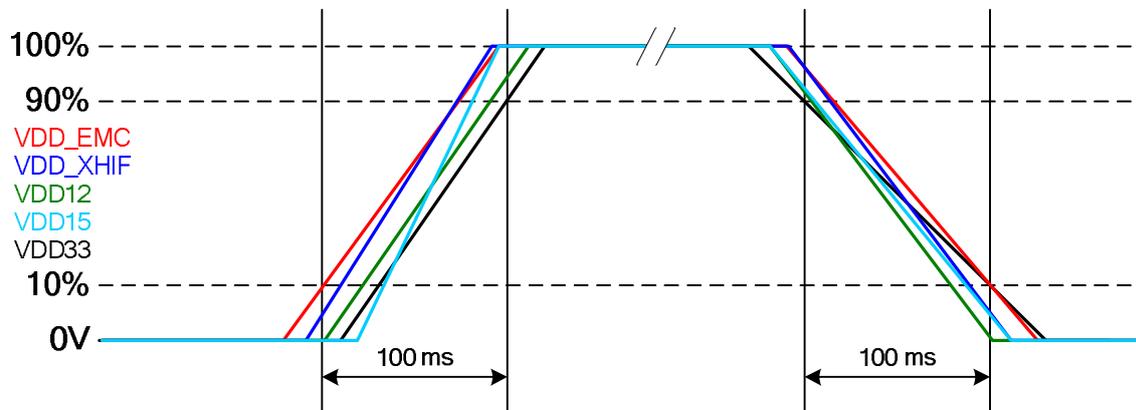


Figure 11: Power Sequence example

An order for the turning on / off of the supply voltages is not prescribed. All voltages must reach their value within a common timeslot of 100 ms.

Attention! To ensure high impedance on the outputs during start of the supply voltages the inputs CTRL_STBY0-2 must tied to '0' in this time (associated with XRESET). Be aware that the three pins influence paths with 3.3 and 1.8/3.3 V as well. The connected signals must have corresponding voltages with 3.3 and 1.8 V.

- CTRL_STBY0 (controls GPIO31:0): 3.3V
- CTRL_STBY1 (controls GPIO92:32 / XHIF³): 1.8V/3.3V
- CTRL_STBY2 (controls GPIO95:32 / XHIF⁴): 1.8V/3.3V

³ Pins connected to CTRL_STBY1:

- GPIO(79-64; 62-46; 44-32) or
- XHIF_D(28; 15-0) / _BE(2-0) / _A(19-15; 13-0) / _SEG_2-0 / _XRDY / _XIRQ / _XWR / _XRD / _XCSR_A_20 / _XCS_M

⁴ Pins connected to CTRL_STBY2

- GPIO(95-93; 91-80; 63; 45) or
- XHIF_D(31-29; 27-16) / _BE(3) / _A(14)

6.2 ERTEC 200P Design recommendations

6.2.1 Design recommendations for ERTEC 200P EMC Bus

6.2.1.1 Possible ERTEC 200P EMC configurations

The EMC configuration is application depending, the pictures below show all possible configurations.

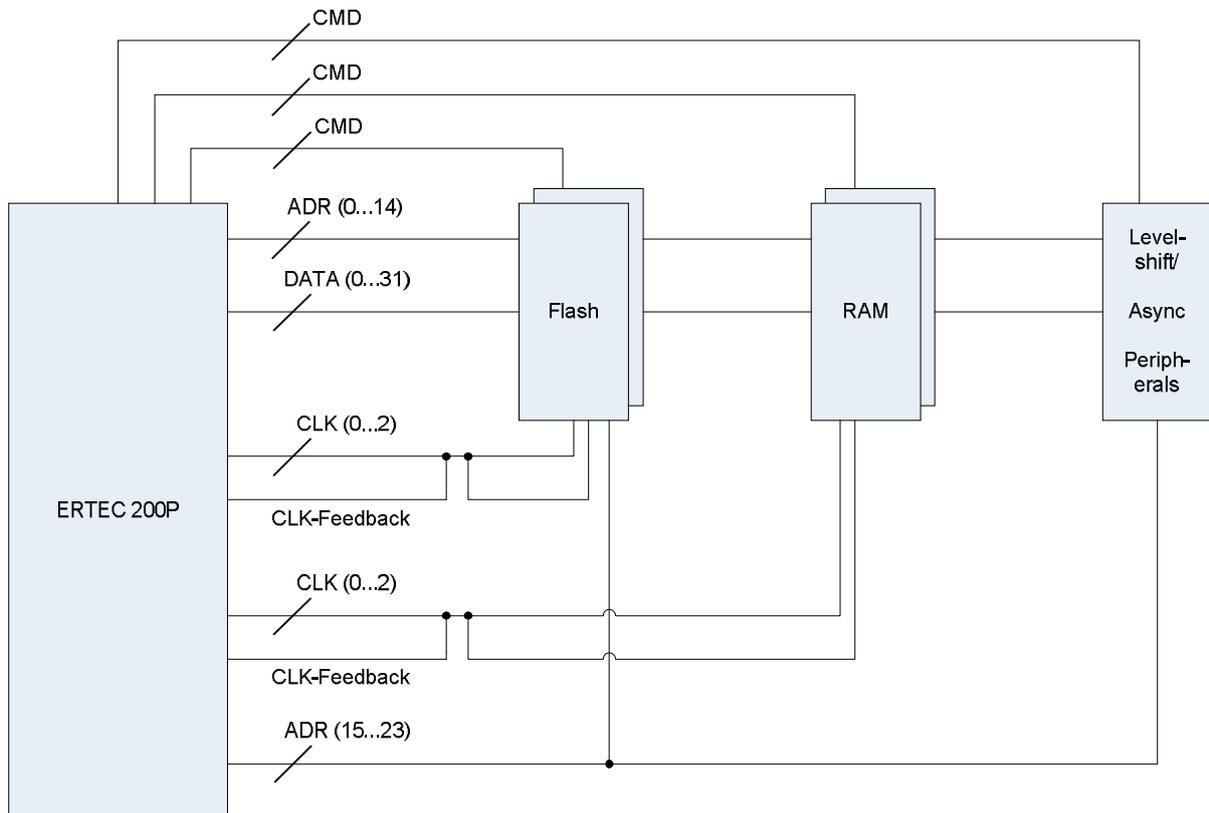


Figure 12: EMC Bus configurations

Allowed velocity and impedance on all transmission lines

	velocity ($\mu\text{m} / \text{ps}$)	Impedance (ohm)
typical	150	60
bestcase	182	69
worstcase	137	51

Table 18: Velocity/ impedance on traces

6.2.1.2 ERTEC 200P EMC recommendations

The recommended values below full fill all these bus configurations/ requirements for ERTEC 200P:

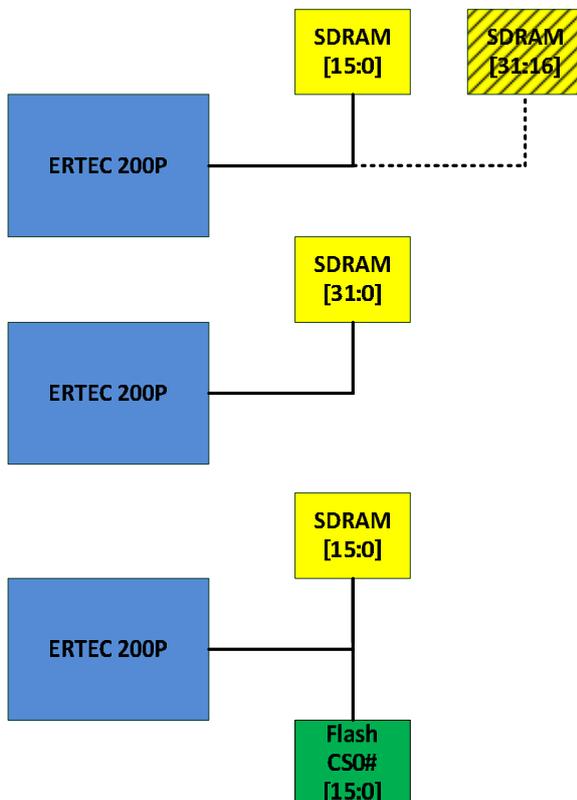
- Min/Max length configuration from driver to receiver

	Max length [mm]	Min length [mm]	Max Vias
Adress [0-14]	87	6	5
Adress [15-23]/ CMD	84	6	4
Data	114	17	4
Clock/ CMD-DQMs	80	17	2

Table 19: Min/ max trace length

- All transmission lines should be routed on inner layers and referenced to Ground.
- All Clocks to SD-RAM and the associated feedback clock to ERTEC 200P must be length matched within 1mm.
- All Clocks to Flash and the associated feedback clock to ERTEC 200P must be length matched within 1mm.
- Clocks must always be routed as short as possible.
- Length matching between Data and Adress to their corresponding clocks is not necessary.
- Clock must be shorter as shortest Data line.
- If Address is below 17mm, clock max length is 17mm (corner case).

Usecase “External Host”



- In the case where just one participant is on ADR (address), Data or CMD/CTR line (see above) an additional 8,2pF capacitor is necessary on SDRAM signal lines (take care on dedicated SDRAM signals).

6.2.1.3 Controlling of an external Level-Shifter

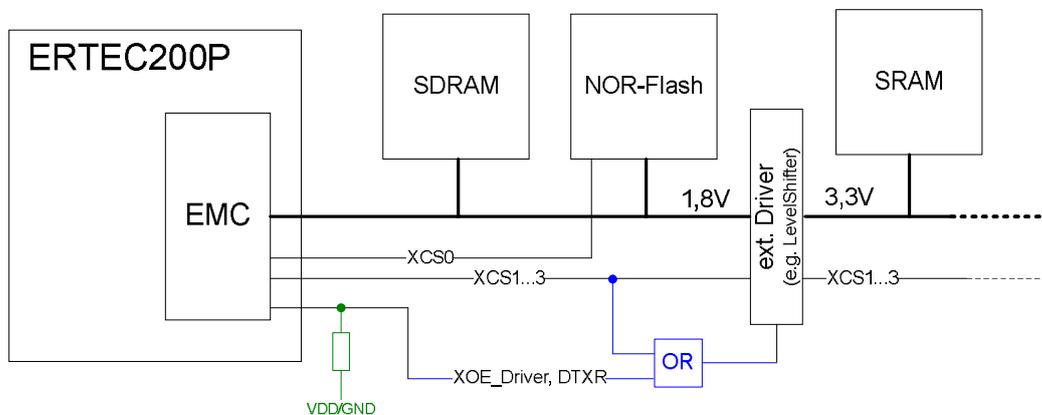
The external Level-Shifter can be controlled by the signals DTXR and XOE_DRIVER on the EMC-Interface. The signals can only be used for the asynchronous memories. The usage of the signals is optional.

The control signals (DTXR and XOE_DRIVER) for the Level-Shifter will be activated independent of the respective address area of the asynchronous EMC-Interface (CS0-CS3) and not particular to the chip select.

At accesses to a memory before or after the Level-Shifter the memories at both sides of the Level-Shifter will be active.

This leads to the situation that two participants drive the data bus of the EMC.

To prevent this situation an appropriate logic (marked in blue) has to be integrated, see figure bellow.



Note:

It is necessary to use appropriate pull resistors, signed in green, because the signals DTXR and XOE_DRIVER will be latched at reset for the boot information.

6.2.2 Design Recommendations ERTEC 200P supply voltages pins

see also Chapter 2.2

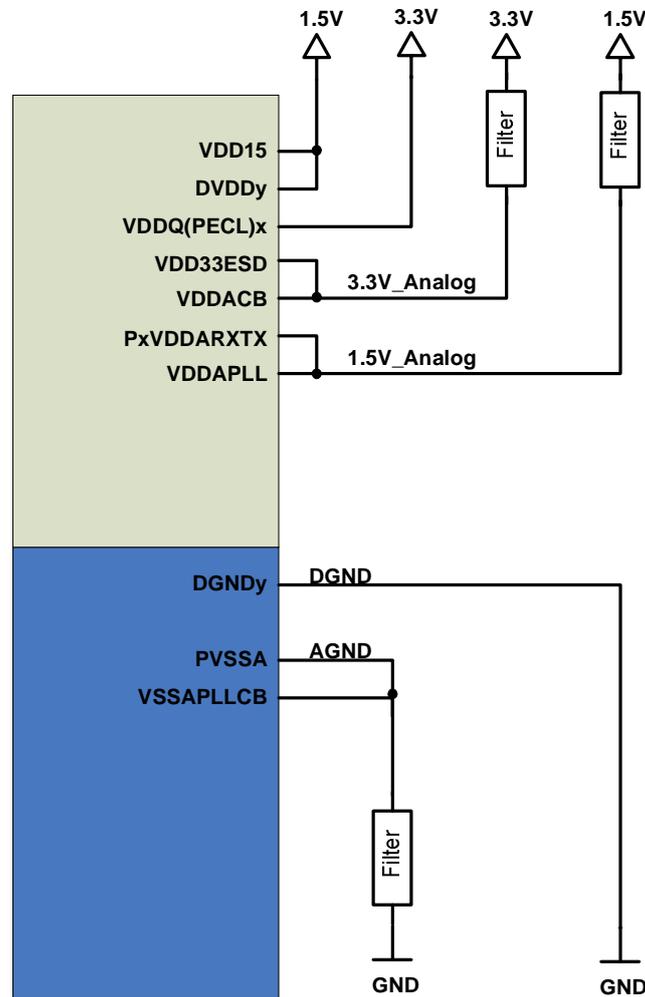
6.2.3 Design Recommendations for ERTEC 200P Profinet PHYs

6.2.3.1 ERTEC 200P PHY supply voltages pins

see also Chapter 2.2

6.2.3.2 Filtering on ERTEC 200P PHY supply voltages

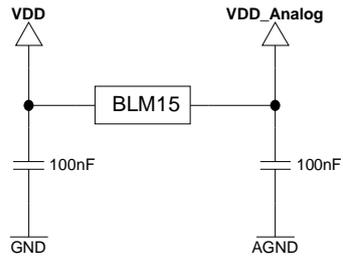
It is recommended to use one power filters (PI-Filters) for **VDD33ESD**, **VDDACB** and an additional one for **PxVDDARXTX**, **VDDAPLL**. The GND pins **PVSSA** and **VSSAPLLCB** should also be separated by a power filter or connected to digital ground at far end from ERTEC 200P.



Note: x = 1,2; y = 1,3

Figure 13: PHY power filtering

Recommended PI-Power filter:



Ceramic Capacitors are $\pm 20\%$
 Ferrite Bead 150Ohm @ 100Mhz

Figure 14: PI Filter

6.2.3.3 Decoupling on ERTEC 200P PHY supply voltages

It is recommend to use three types of decoupling capacitors as shown. The red pair of 10nF and 22nF should be placed as close as possible to **DVDD1**, **DVDD3**, **VDD33ESD**, **VDDACB**, **P1VDDARXTX**, **P2VDDARXTX** and **VDDAPLL**.

The orange pair of 100nF and 22uF should be placed once to the net for **DVDD1/3**, **VDDESD/VDDACB** and **P1VDDARXTX/ P2VDDARXTX/ VDDAPLL**.

The blue 100nF capacitor (shown in blue) should be placed as close as possible for all remaining pins **VDD15** and **VDDQ(PECL)1/2** to the pins.

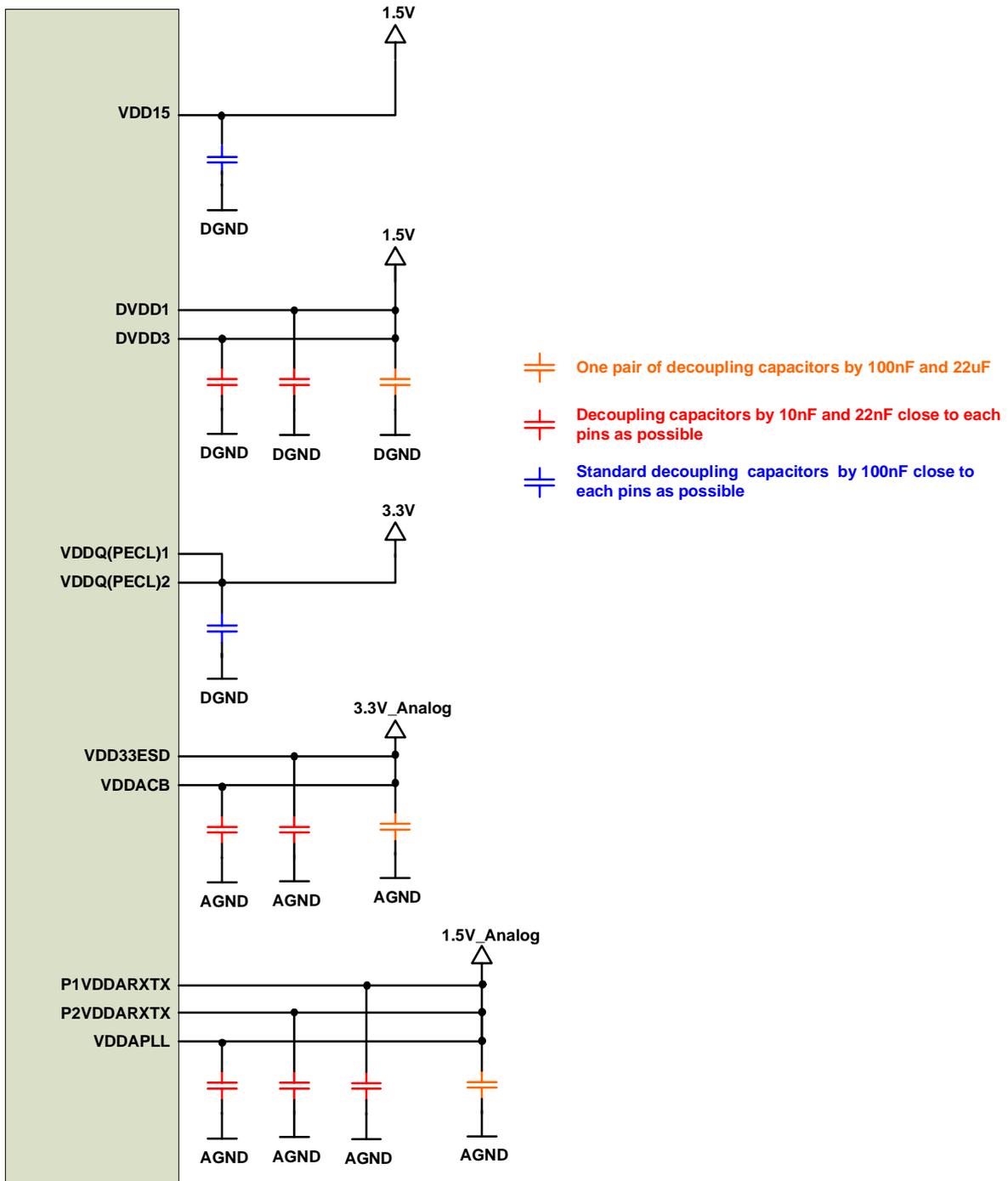
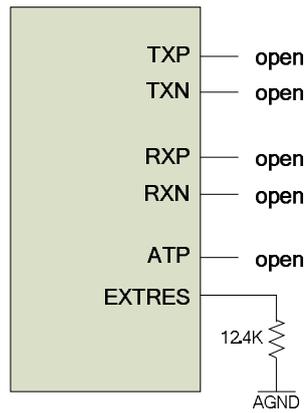


Figure 15: PHY decoupling

6.2.4 ERTEC 200P PROFINET TX circuit

Following design hints are recommended for the UTP interface:

- RX and TX pairs must be routed 100Ohm differential
- Differential length for each pair must match in length
- Transformer must be placed as close as possible to the ERTEC 200P
- Centre Tap of transformer must be connected with 10Ohm series resistor to 3.3V_Analog.



Resistors in black are +/-1% 1/16W

Figure 17: UTP circuit unused

6.2.5 ERTEC 200P PROFINET FX circuit

Following design hints are recommended for the FX interface:

- It is strongly recommended to use PROFINET compliant POF Transceiver QFBR-5978AZ from company Avago.
- RX and TX pairs (LVPECL) must be routed 100Ohm differential
- Differential length for each pair must match in length
- Transceiver must be placed as close as possible to the ERTEC 200P
- 150Ohm series resistors in TX path must be placed as close as possible to the ERTEC 200P
- The RX termination (130Ohm pull up and 82Ohm pull down) must be placed as close as possible to ERTEC 200P
- RX and TX Power supply on transceiver should separately filtered, see datasheet transceiver.
- Care must be taken on level translation between transceiver SD pin and ERTEC 200P PHY input, see recommended circuit below.
- Signals must be placed referenced to digital ground plane or common plane and must be not coupled with other signals.
- Don't connect analog VDD/ AGND (related pins on ERTEC 200P: VDD33ESD, VDDACB/ PVSSA, VSSPLLCB) to FX circuit.

The picture below shows the recommended FX circuit:

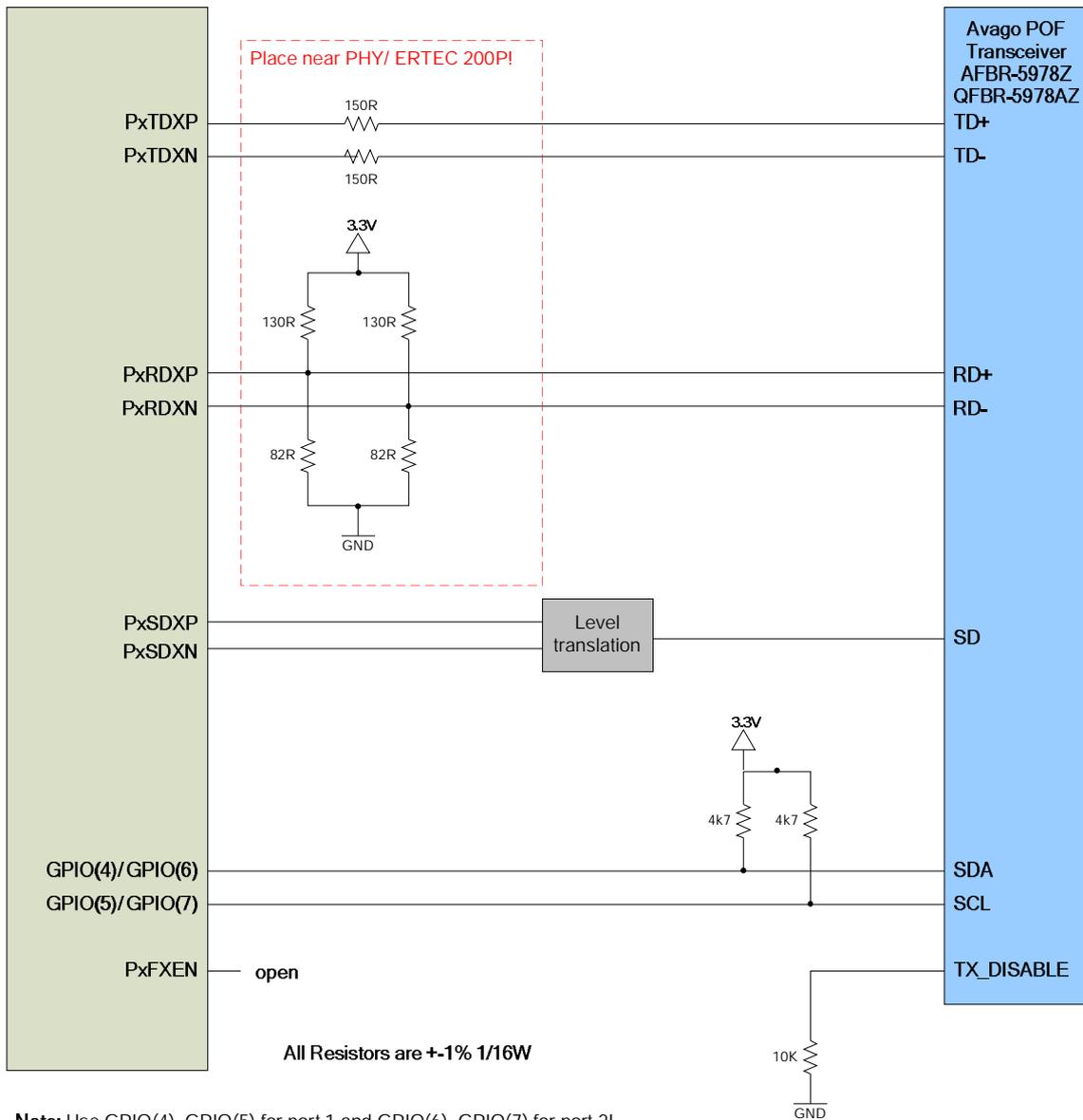


Figure 18: FX circuit

6.2.5.1 ERTEC 200P/ Avago QFBR-5978AZ SD circuit

The Avago QFBR-5978AZ has a single ended output and ERTEC 200P has a differential LVPECL input, following level translation circuit is recommended.

Comparator should be placed near transceiver and PECL driver near ERTEC 200P. The 3,3V supply voltage tolerance for **POF transceiver and SD level translation circuit** is limited to +- 5%.

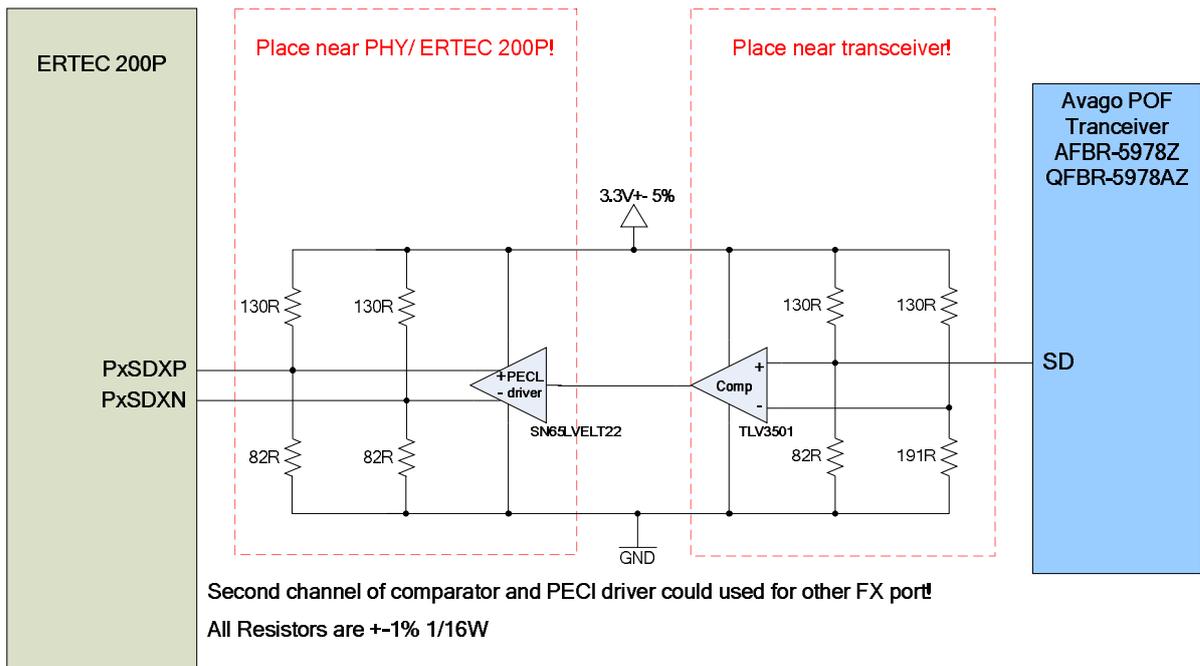


Figure 19: SD level translation circuit

6.2.5.2 ERTEC 200P PROFINET FX circuit unused pins

PxTDXP/N Signals on unused FX port should be left open, **PxRDXP/N** and **PxSDXP/N** inputs should directly connected to GND, the GPIOs could be used for alternate function.

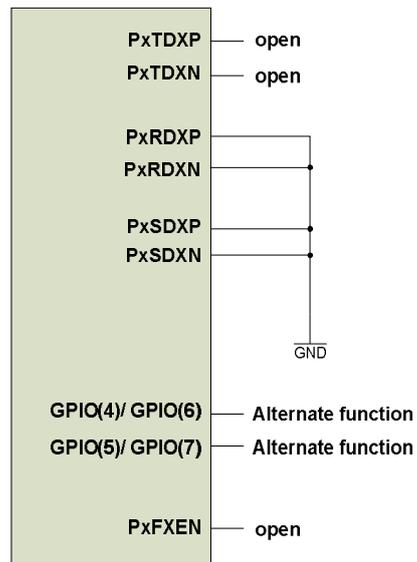
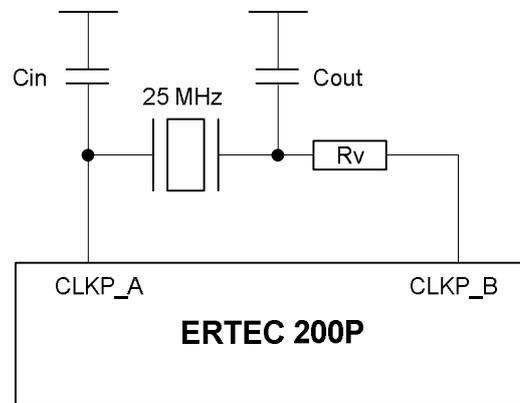


Figure 20: FX circuit unused pins

6.3 Clocking

6.3.1 Oscillator



*Hint:
The input capacitance of the integrated oscillator in the ERTEC 200P is **4.2pF** (including the influence of the package)*

Figure 21: Oscillator Circuitry

Example for an oscillator crystal:

Crystal	Frequency	Rv	Cin	Cout
EPSON TSX-3225	25.00 MHz	22 Ω	15 pF	15 pF

Note that the oscillator frequency must be at least 25 MHz, otherwise the PLL will not operate properly.

PCB layout hints:

- Place the input and output pins of the oscillator and the resonator and external components close to each other, and keep wiring as short as possible.
- Make the wiring between the ground side of the capacitor and the ground pin of the ERTEC 200P as short and as thick as possible.
- Keep the lead wire of the resonator and capacitor as short as possible, and fix the resonator and capacitor to the printed circuit board to keep the influence of mechanical vibrations to a minimum.
- Layout the external components so that they are surrounded by GND as far as possible.

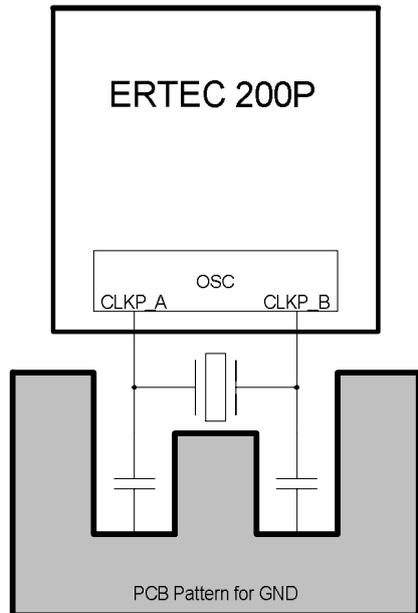


Figure 22 : Oscillator Circuitry Layout Example

6.3.2 External clock source

It is possible to use an external clock source instead of a quartz crystal as clock input for port CLKP_A as well. In this case the Port CLKP_B has to be left unconnected (open) and the port CLKP_A has to fulfill the following requirements:

Parameter	Description	Min	Typ	Max	Unit
f_{IN}	external clock source frequency	¹⁾	25	¹⁾	MHz
V_{IH}	CLKP_A high level voltage	2	3,3	VDDACB	V
V_{IL}	CLKP_A low level voltage	0	-	0,8	V
t_{RFC}	CLKP_A rise or fall time	0	1	4	ns
t_w	CLKP_A high or low time	16 ²⁾	20 ²⁾	24 ²⁾	ns
t_{JIT}	CLKP_A jitter tolerace	-	20	-	ps (RMS)
DuCy	CLKP_A duty cycle	40	50	60	%

¹⁾ +/- 50ppm over the whole lifetime and temperature range

²⁾ t_w was calculated at $f_{IN(TYP)} = 25\text{MHz}$, e.g. $t_{w(MIN)} = 10^* (DuCy_{(MIN)} / f_{IN(TYP)})$

6.3.3 PLL Power Supply

Since GND noise may affect VDD through C1 and C2, GND must be stable.

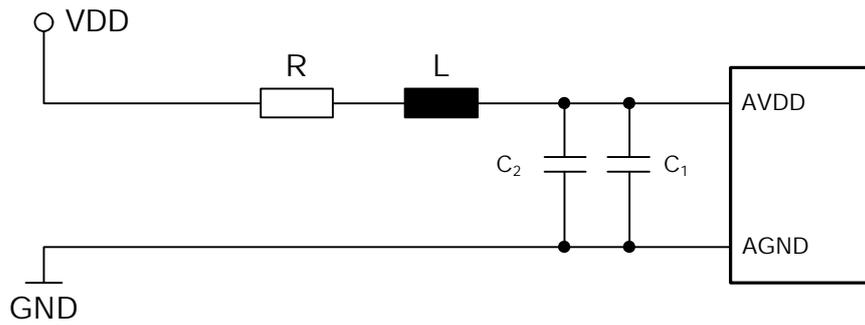


Figure 23: Recommended for PLL Power Supply Filter

Dimensioning the PLL Power Supply Filter

$$\xi = \frac{R + R_L}{2} \cdot \sqrt{\frac{C_1 + C_2}{L}} \quad (\text{damping factor})$$

$$f_0 = \frac{1}{2\pi \sqrt{L \cdot (C_1 + C_2)}} \quad (\text{cut off frequency in Hz})$$

where $R + R_L \leq 0.8 \Omega$, $C_2 \geq 10 \mu\text{F}$, $\xi \approx 0.7$ (should not be less than 0.7 to decrease the sensitivity for resonance), $f_0 \leq 5\text{kHz}$

Example:

With $R + R_L = 0.8 \Omega$, $L = 22 \mu\text{H}$, $C_2 = 68 \mu\text{F}$, $C_1 = 0.3 \mu\text{F}$ (ceramic capacitor) this results in $f_0 = 4.1 \text{ kHz}$ and $\xi = 0.70$.

C_1 should be an SMD capacitor (e.g. ceramic 300 nF) for elimination of high frequency components. Be sure to place it as close as possible to a power supply pin.

6.4 Reset

The minimal duration for reset is shown in the table below.

Parameter	Symbol	Min	Typ	Max	Unit
Reset pulse width ¹⁾	t _{RES1}	30			µs
Reset pulse width ²⁾	t _{RES2}	40			ns

¹⁾ Applies to pin XRESET during power-up phase (accounts for oscillator start-up time)

²⁾ Applies to pins XSRST and XTRST for operating, powered-up ASIC (oscillator is running)

Table 20: Minimal reset duration

6.4.1 Power-On Reset Behaviour

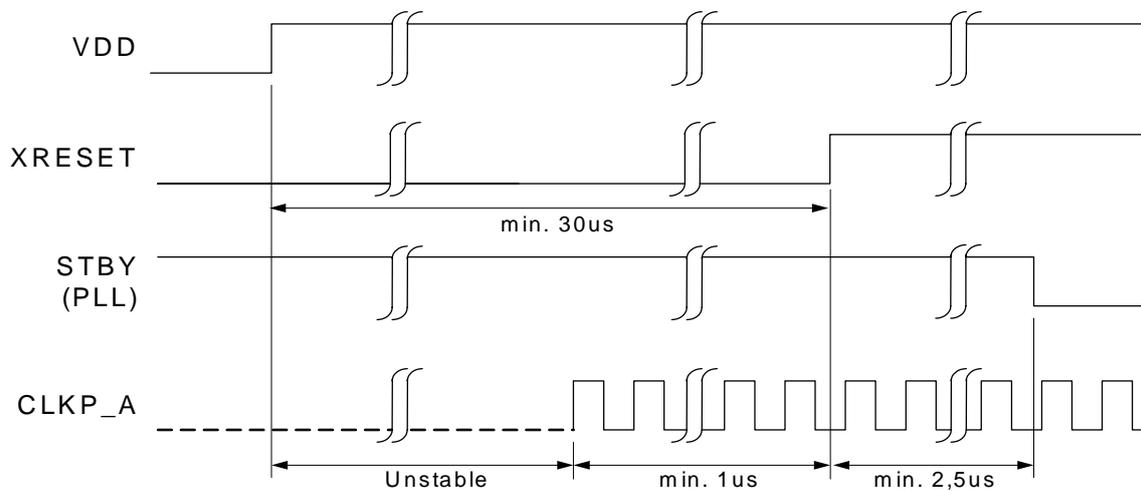
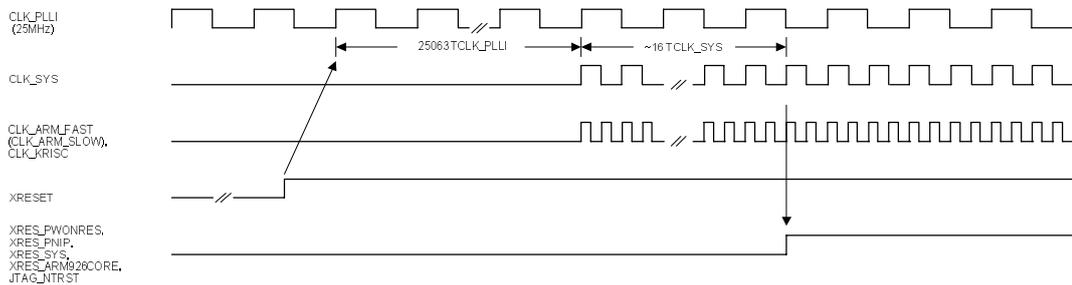


Figure 24: Power-On Reset Behaviour

Timing power up reset



Timing watchdog / software reset

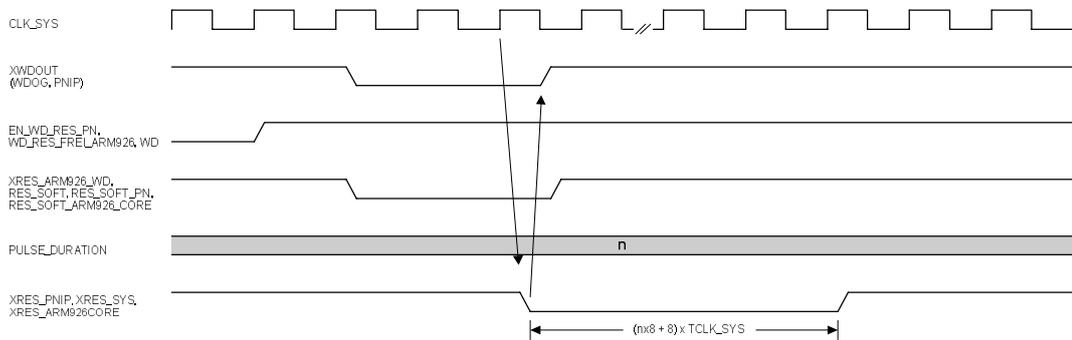


Figure 25: Timing reset

On access, e.g. over the XHIF-Interface, to internal resources of the ERTEC 200P directly after release of XRESET is to mention, that they are only allowed after the internal initialisation is finished (see also StartUp-Times in Chapter 7.7.1)

Duration of initialisation after deactivating the XRESET:

PLL-Standby-Time:	32,5 μs
PLL-Lockup-Time:	1002,5 μs
EMC Init Done ¹⁾ :	233,0 μs
Complete-Time:	1268,0 μs

¹⁾ Parallel to the EMC Init_Done several internal SRAMs are also initialised in this time. The time for the EMC Init_Done is the biggest. Therefore it is listed here.

6.4.2 Strapping Pins

During XRESET is active, the Input-Value for the Config- and Boot-Pins are LATCHED in. After XRESET is released, the values are stored. The values on the Config- and Boot-Pins must stay stable 120ns after the XRESET is released. See Chapter 7.6 and 7.7 for more details

6.4.3 Reset Structure

6.4.3.1 Asynchronous PowerOn-Reset

The asynchronous⁵ PowerOn-Reset is connected via the Pin XRESET to the ERTEC 200P. As reaction to this reset the complete circuit (incl. Clock-system) of the ERTEC 200P is reset and the Configuration- and Boot-Pins are latched (see Chapter 0). The PowerOn-Reset must stay active for at least 30 μs after the supply-voltages are supplied. Afterwards the PLL ramps up and is locked 1000 μs later. The time until lock of the PLL is called t_{LOCK} . The PowerOn-Reset-Phase is internally enlarged for this time (PLL-Lock is not interpreted) and the Clock-system is connected at the end of the rampup-phase. The internal reset stays active for additional 16 Clocks to reset the internal logic. A communication of the debugger over the JTAG-interface is not possible at this time.

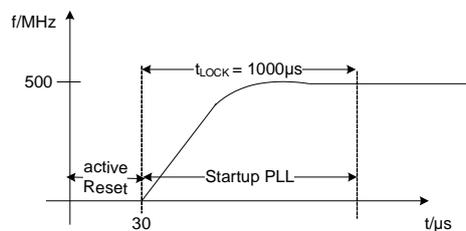


Figure 26: StartUp of the PLL

The lock-state of the PLL is monitored by a hardware. The IRQ49 interrupt announces whether the PLL has lost its input clock (quartz break) or the PLL is not locked (PLL-Monitor, monitors input- to output-frequency). Additionally the two Error-states can be polled from the SCRB-Register 'PLL_STAT_REG'.

An integrated filter of the ERTEC 200P ensures that spikes $\leq 40\text{ns}$ (bestcase) on the input XRESET are eliminated.

In order to analyse the Reset-Source after a restart, the Bit PWRON_HW_RES of the Register RES_STAT_REG is set on PowerOn-Reset. On restart the software can read the Register RES_STAT_REG.

6.4.3.2 Asynchronous Hardware-Reset

The hardware-reset is activated over the Pin XSRST from an external debugger. XSRST is a bidirectional IO-cell with Open-Drain output. During the active XSRST-Phase the complete internal logic is reset, but not the Clock-system. Additionally the configuration-pins are not latched. During the Hardware-Reset-Phase the debugger can communicate over the JTAG-Interface with the embedded ICE Logic, e.g. to load a breakpoint. Thereby a single-stepping from the reset-address is possible.

An integrated filter of the ERTEC 200P ensures that spikes $\leq 40\text{ns}$ (bestcase) on the input XSRST are eliminated.

In order to analyse the Reset-Source after a restart, the Bit PWRON_HW_RES of the Register RES_STAT_REG is set on PowerOn-Reset. On restart the software can read the Register RES_STAT_REG.

On Reboot after a hardware-reset the system uses the bootmode which was latched during the PowerOn-Reset.

XSRST is activated to the debugger if PowerOn-Reset is active. It is forbidden to activate XSRST during a 'RES_SOFT_ARM926_CORE' is active! The Debugger won't run **during** if the core is in reset.

6.4.3.3 Asynchronous JTAG-Reset

The JTAG-Reset is activated through the Pin XTRST from the external debugger. Only the embedded ICE logic of the ARM926EJ-S is reset. To ensure a defined state of the embedded ICE logic without using a debugger, the logic is also resetted during PowerOn-Reset (XRESET).

An integrated filter of the ERTEC 200P ensures that spikes $\leq 40\text{ns}$ (bestcase) on the input XTRST are eliminated. Normally a spike on XTRST is not passed to the JTAG Controller. A sequence is therefore necessary on TDI/TMS and TCK.

⁵ The asynchronous Reset acts on the Reset-Input of a Flip-Flop. The Reset is assigned asynchronous but released synchronous.

Hint for board-layout:

Instructions for external Pull-Resistors on XTRST can be found in Chapter 2.1.4

6.4.3.4 Asynchronous ARM926 Watchdog-Reset

The ARM926 Watchdog-Reset forms a hardware observation of the software from the ARM926EJ-S. The base for the observation is a time which is adjustable in the watchdog-timer. On activation of the watchdog the time counts. If no retrigger is done within this time, the watchdog-reset (XRES_ARM926_WD) is triggered (output ARM926 watchdog: WD_XWDOUT1). If the watchdog-function is enabled (WD_RES_FREI_ARM926) the ERTEC 200P is reset. In order to analyse the Reset-Source after a restart, the Bit ARM926_WDOG_RES of the Register RES_STAT_REG is set on PowerOn-Reset. The Bit keeps set from the reset-function. On restart the software can read the Register RES_STAT_REG.

For application, in which the expiration of the watchdog should have no negative effect on the PN-IP, the PN-IP can be excluded from the reset per watchdog (EN_WD_RES_PN = 0 in ASYN_RES_CTRL_REG).

Attention: The Bit EN_WD_RES_PN is always set if the PN-IP is reset! If an asynchronous software-reset is generated from the software for the PN-IP, the software has to set EN_WD_RES_PN = 0 if the Watchdog-Reset of the ARM926 should have no effect to the PN-IP.

In advance to the watchdog expiration an interrupt 'WD_INT_ARM926' is generated to the ARM926 and to an external host the watchdog expiration is advanced with 'WD_XWDOUT0' over a GPIO-Pin.

The watchdog also expires if the clock-generation fails (e.g. quartz break). The PLL enters his free-running-frequency in this case (100 – 300 MHz).

On Reboot after a Watchdog-Reset the system uses the bootmode which was latched during the PowerOn-Reset.

6.4.3.5 Asynchronous Software-Reset for the ERTEC 200P (without PN-IP)

In the ERTEC 200P an asynchronous Software-Reset can be generated by setting the Bit 'RES_SOFT' in the Register RES_CTRL_REG. The PN-IP and the PHYs are not reset in this case. In order to analyse the Reset-Source after a restart, the Bit SW_RES of the Register RES_STAT_REG is set on Software-Reset. The Bit keeps set from the reset-function. On restart the software can read the Register RES_STAT_REG.

On Reboot after a hardware-reset the system uses the bootmode which was latched during the PowerOn-Reset.

6.4.3.6 Asynchronous Software-Reset of the PN-IP

The PN-IP and the PHYs can be reset separately from Software by setting the Bit 'RES_SOFT_PN' in the SCRB-Register 'ASYN_RES_CTRL_REG'.

The HW-Reset for the integrated PHYs comes from 'phy_reset_o' output of the PN-IP. If the SMI-Modul of the PN-IP is not active (configuration-mode) the 'phy_reset_o' output is active and keeps the PHYs in reset-state.

A simultaneous SW-Reset for the ERTEC 200P and the PN-IP reset the complete ERTEC 200P.

6.4.3.7 Asynchronous Software-Reset of the ARM926EJ-S Core

The ARM926EJ-S Core (without TCM926) has its own reset, which can be generated by setting the Bit 'RES_SOFT_ARM926_CORE' in the SCRB-Register 'ASCN_RES_CTRL_REG'.

'RES_SOFT_ARM926_CORE' acts only to the ARM926EJ-S Core System and not to the TCM_Block_926. The TCM_Block_926 is reset with XRESET, XSRST, XRES_ARM926_WD or RES_SOFT.

In order to analyse the Reset-Source after a restart, the Bit SW_RES_ARM926 of the Register RES_STAT_REG is set on Software-Reset. The Bit keeps set from the reset-function. On restart the software can read the Register RES_STAT_REG.

The asynchronous Software-Reset for the ARM926EJ-S Core is necessary after the Bootloader has adjusted the final TCM926 configuration. Only with reset the ARM926EJ-S uses the TCM926 configuration (DRSIZE for D-TCM and IRSIZE for I-TCM configured in Register TCM926_MAP).

6.4.3.8 Synchronous Software-Reset (PN-IP, PER-IF, Hostinterface)

The PN-IP, the Peripherie-Interface or the Host-Interface can also be reset from Software in the SCRB-Register 'SYN_RES_CTRL_REG' synchronously. This synchronous resets work on the SYN-

Reset Inputs of the corresponding IPs and resets only the State-Machines and local registers, but not the parameterization-Registers and the AHB-Interface. The SW has to set the corresponding Bits in the Register 'SYN_RES_CTRL_REG' and reset them afterwards. With this function the software can control on it own the reset-state of the modules (short impulse: dyn. reset, constant '1': disable-state).

6.5 GPIO Pins

The GPIO layer mainly provides means for flexible I/O pin mapping / routing. By use of multiplexers it is possible to obtain variable interconnections between predefined signal groups and ASIC I/O pins.

The structure of a single GPIO cell is shown below in Figure 27. Each cell can either be used for I/O pin routing or as input / output pin of the GPIO parallel ports.

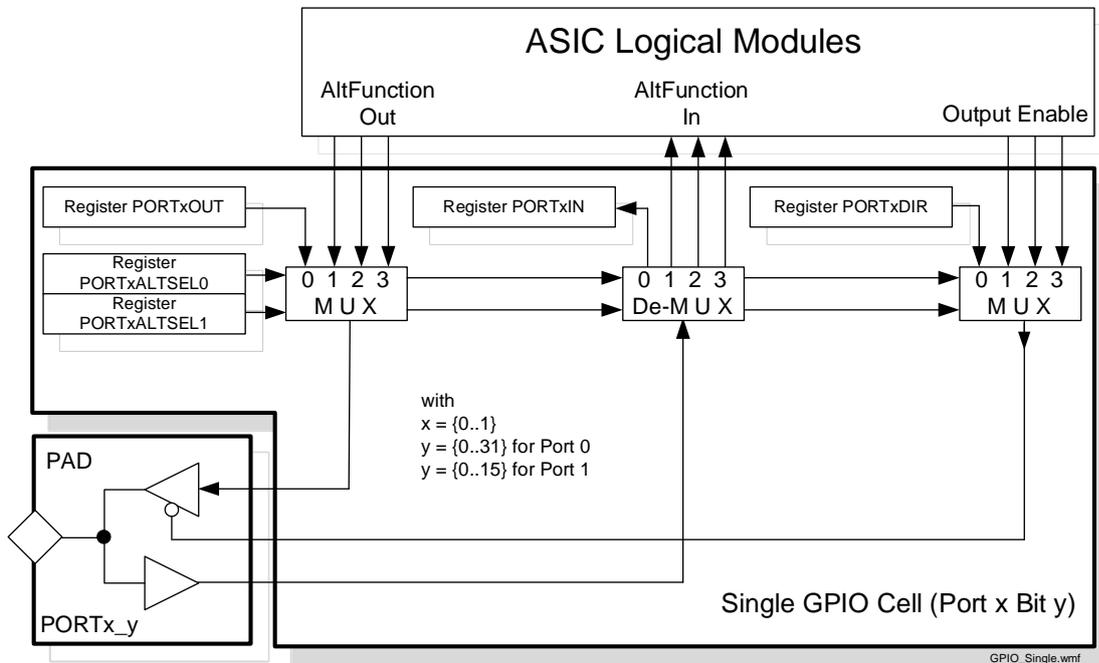


Figure 27: Single GPIO Cell

For I/O pin routing, one of 3 alternative functions can be selected for each GPIO cell (see Chapter 7.5 for GPIO pin mapping).

6.6 Pull-Up / Pull-Down Resistors

The Renesas' specifications for pull-up and pull-down resistors are listed in the table below.

Resistor Type	Min	Typ	Max	Unit
50 k Ω pull-up (3.3 V buffer)	40.5	51.9	70.1	k Ω
50 k Ω pull-up (1.8 V buffer)	38.6	49.7	66.9	k Ω
50 k Ω pull-down (3.3 V buffer)	37.0	49.6	70.4	k Ω
50 k Ω pull-down (1.8 V buffer)	35.8	47.6	66.4	k Ω

Table 21: Pull-Up / Pull-Down Resistor Values

Since the maximum values of the internal pull-ups / pull-downs can be rather high in worst case, critical inputs (resets etc.) must not rely on the internal resistors but must be supplied with external pull-up / pull-down resistors.

When combining external pull-up resistors with internal pull-down resistors (and vice versa) the following recommendation should be considered:

- A 50k internal pull-up (at its minimum value) combined with a 4k7 pull-down results in a maximum logic low level V_{IL} of 0.36 V ($V_{DD} = 3.5$ V, required: $V_{IL} \leq 0.8$ V).

- A 50k internal pull-down (at its minimum value) combined with a 10k pull-up results in a minimum logic high level V_{IL} of 2.36 V ($V_{DD} = 3.0$ V, required: $V_{IH} \geq 2.0$ V).

As a rule of thumb the values of the external resistors should not be higher than those listed above. Note that external components connected to a GPIO pin may have other switching thresholds and additional pull-up resistors which will reduce the effective pull-up resistor value on that GPIO pin.

6.7 Debug

The debugging with the JTAG-Interface is described in /1/

7 Basic Configuration

7.1 Address Map

A description can be found in /1/

7.2 Interrupts

A description can be found in /1/

7.3 DMA Requests

A description can be found in /1/

7.4 Timers

A description can be found in /1/

7.5 GPIO Pin Mapping

GPIO Pin	GPIO Registers	GPIO Alternative Function A	GPIO Alternative Function B	GPIO Alternative Function C
GPIO0_INT	GPIO_*_0.0	PNPLL_OUT0_a	TIM_OUT0_a	NOT_USED
GPIO1_INT	GPIO_*_0.1	PNPLL_OUT1_a	TIM_OUT1_a	NOT_USED
GPIO2_INT	GPIO_*_0.2	PNPLL_OUT2_a	TIM_OUT2	DBGCRQ
GPIO3_INT	GPIO_*_0.3	PNPLL_OUT3_a	TIM_OUT3	DBGACK
GPIO4_INT	GPIO_*_0.4	PNPLL_OUT4_a	TIM_OUT4	I2C_SDO1_1_a
GPIO5_INT	GPIO_*_0.5	PNPLL_OUT5_a	TIM_OUT5	I2C_SCLK_1_a
GPIO6_INT	GPIO_*_0.6	PNPLL_OUT6_a	TIM_TRIG0_a	I2C_SDO1_2_a
GPIO7_INT	GPIO_*_0.7	PNPLL_OUT7_a	TIM_TRIG1_a	I2C_SCLK_2_a
GPIO8_INT	GPIO_*_0.8	PNPLL_OUT8_a	TIM_TRIG2	SPI_2_SCLKIN_b
GPIO9_INT	GPIO_*_0.9	PNCLKA_IN_a	TIM_TRIG3	SPI_2_SFRMIN_b
GPIO10_INT	GPIO_*_0.10	NOT_USED	TIM_TRIG4	SPI_2_SSPOE_b
GPIO11_INT	GPIO_*_0.11	PNTIME_OUT_a	TIM_TRIG5	SPI_2_SSPECTLOE_b
GPIO12_INT	GPIO_*_0.12	PNTIME_IN	U2_CTS	SPI_2_SCLKOUT_b
GPIO13_INT	GPIO_*_0.13	WD_XWDOUT0_a	U2_RTS	SPI_2_SFRMOUT_b
GPIO14_INT	GPIO_*_0.14	I2C_SCLK_3	U2_TXD	SPI_2_SSPTXD_b
GPIO15_INT	GPIO_*_0.15	I2C_SDO1_3	U2_RXD	SPI_2_SSPRXD_b
GPIO16	GPIO_*_0.16	SPI_1_SCLKOUT_a	NOT_USED	NOT_USED
GPIO17	GPIO_*_0.17	SPI_1_SFRMOUT_a	NOT_USED	NOT_USED
GPIO18	GPIO_*_0.18	SPI_1_SSPTXD_a	NOT_USED	NOT_USED
GPIO19	GPIO_*_0.19	SPI_1_SSPRXD_a	NOT_USED	NOT_USED
GPIO20	GPIO_*_0.20	SPI_1_SSPOE_a	NOT_USED	NOT_USED
GPIO21	GPIO_*_0.21	SPI_1_SSPECTLOE_a	NOT_USED	NOT_USED
GPIO22	GPIO_*_0.22	SPI_1_SFRMIN_a	NOT_USED	NOT_USED
GPIO23	GPIO_*_0.23	SPI_1_SCLKIN_a	PNCLKA_IN_b	NOT_USED
GPIO24	GPIO_*_0.24	SPI_2_SCLKOUT_a	TIM_OUT0_b	NOT_USED
GPIO25	GPIO_*_0.25	SPI_2_SFRMOUT_a	TIM_OUT1_b	NOT_USED
GPIO26	GPIO_*_0.26	SPI_2_SSPTXD_a	TIM_TRIG0_b	NOT_USED
GPIO27	GPIO_*_0.27	SPI_2_SSPRXD_a	TIM_TRIG1_b	NOT_USED
GPIO28	GPIO_*_0.28	SPI_2_SCLKIN_a	U3_TXD	PNTIME_OUT_b
GPIO29	GPIO_*_0.29	SPI_2_SFRMIN_a	U3_RXD	PNPLL_OUT6_b
GPIO30	GPIO_*_0.30	SPI_2_SSPOE_a	NOT_USED	PNPLL_OUT7_b
GPIO31	GPIO_*_0.31	SPI_2_SSPECTLOE_a	NOT_USED	PNPLL_OUT8_b

Table 22: GPIO Port 0 Input Mapping

GPIO Pin	GPIO Registers	GPIO Alternative Function A	GPIO Alternative Function B	GPIO Alternative Function C
XHIF_A1	GPIO_*_1.0	NOT_USED	NOT_USED	NOT_USED
XHIF_A2	GPIO_*_1.1	NOT_USED	NOT_USED	NOT_USED
XHIF_A3	GPIO_*_1.2	NOT_USED	NOT_USED	NOT_USED
XHIF_A4	GPIO_*_1.3	NOT_USED	NOT_USED	NOT_USED
XHIF_A5	GPIO_*_1.4	NOT_USED	NOT_USED	NOT_USED
XHIF_A6	GPIO_*_1.5	NOT_USED	NOT_USED	NOT_USED
XHIF_A7	GPIO_*_1.6	NOT_USED	NOT_USED	NOT_USED
XHIF_A8	GPIO_*_1.7	NOT_USED	NOT_USED	NOT_USED
XHIF_A9	GPIO_*_1.8	NOT_USED	NOT_USED	SPI_1_SCLKOUT_b
XHIF_A10	GPIO_*_1.9	NOT_USED	NOT_USED	SPI_1_SFRMOUT_b
XHIF_A11	GPIO_*_1.10	NOT_USED	NOT_USED	SPI_1_SSPTXD_b
XHIF_A12	GPIO_*_1.11	NOT_USED	NOT_USED	SPI_1_SSPRXD_b
XHIF_A13	GPIO_*_1.12	NOT_USED	NOT_USED	SPI_1_SSPOE_b
XHIF_A14	GPIO_*_1.13	NOT_USED	NOT_USED	SPI_1_SSPCTLOE_b
XHIF_A15	GPIO_*_1.14	NOT_USED	NOT_USED	SPI_1_SCLKIN_b
XHIF_A16	GPIO_*_1.15	NOT_USED	NOT_USED	SPI_1_SFRMIN_b
XHIF_A17	GPIO_*_1.16	NOT_USED	NOT_USED	U1_CTS
XHIF_A18	GPIO_*_1.17	NOT_USED	NOT_USED	U1_DCD
XHIF_A19	GPIO_*_1.18	NOT_USED	NOT_USED	U1_DSR
XHIF_SEG_2	GPIO_*_1.19	NOT_USED	NOT_USED	U1_RI
XHIF_SEG_0	GPIO_*_1.20	NOT_USED	NOT_USED	U1_RTS
XHIF_SEG_1	GPIO_*_1.21	NOT_USED	NOT_USED	U1_DTR
XHIF_XRDY	GPIO_*_1.22	NOT_USED	NOT_USED	U4_TXD
XHIF_XRQ	GPIO_*_1.23	NOT_USED	NOT_USED	U4_RXD
XHIF_XWR	GPIO_*_1.24	NOT_USED	NOT_USED	PNPLL_OUT0_b
XHIF_XRD	GPIO_*_1.25	NOT_USED	NOT_USED	PNPLL_OUT1_b
XHIF_XCS_R_A20	GPIO_*_1.26	NOT_USED	NOT_USED	PNPLL_OUT2_b
XHIF_XCS_M	GPIO_*_1.27	NOT_USED	NOT_USED	PNPLL_OUT3_b
XHIF_XBE0	GPIO_*_1.28	NOT_USED	NOT_USED	PNPLL_OUT4_b
XHIF_XBE1	GPIO_*_1.29	NOT_USED	NOT_USED	PNPLL_OUT5_b
XHIF_XBE2	GPIO_*_1.30	NOT_USED	NOT_USED	U1_TXD
XHIF_XBE3	GPIO_*_1.31	NOT_USED	NOT_USED	U1_RXD

Table 23: GPIO Port 1 Input Mapping

GPIO Pin	GPIO Registers	GPIO Alternative Function A	GPIO Alternative Function B	GPIO Alternative Function C
XHIF_D0	GPIO_*_2.0	NOT_USED	NOT_USED	NOT_USED
XHIF_D1	GPIO_*_2.1	NOT_USED	NOT_USED	NOT_USED
XHIF_D2	GPIO_*_2.2	NOT_USED	NOT_USED	NOT_USED
XHIF_D3	GPIO_*_2.3	NOT_USED	NOT_USED	NOT_USED
XHIF_D4	GPIO_*_2.4	NOT_USED	NOT_USED	NOT_USED
XHIF_D5	GPIO_*_2.5	NOT_USED	NOT_USED	NOT_USED
XHIF_D6	GPIO_*_2.6	NOT_USED	NOT_USED	NOT_USED
XHIF_D7	GPIO_*_2.7	NOT_USED	NOT_USED	XSSI_DATA
XHIF_D8	GPIO_*_2.8	NOT_USED	NOT_USED	SSI_CLK
XHIF_D9	GPIO_*_2.9	NOT_USED	NOT_USED	SSI_DATA
XHIF_D10	GPIO_*_2.10	NOT_USED	NOT_USED	NOT_USED
XHIF_D11	GPIO_*_2.11	NOT_USED	NOT_USED	WD_XWDOUT0_b
XHIF_D12	GPIO_*_2.12	NOT_USED	NOT_USED	NOT_USED
XHIF_D13	GPIO_*_2.13	NOT_USED	NOT_USED	NOT_USED
XHIF_D14	GPIO_*_2.14	NOT_USED	NOT_USED	NOT_USED
XHIF_D15	GPIO_*_2.15	NOT_USED	NOT_USED	NOT_USED
XHIF_D16	GPIO_*_2.16	NOT_USED	NOT_USED	I2C_SDO1_1_b
XHIF_D17	GPIO_*_2.17	NOT_USED	NOT_USED	I2C_SCLK_1_b
XHIF_D18	GPIO_*_2.18	NOT_USED	NOT_USED	I2C_SDO1_2_b
XHIF_D19	GPIO_*_2.19	NOT_USED	NOT_USED	I2C_SCLK_2_b
XHIF_D20	GPIO_*_2.20	NOT_USED	NOT_USED	NOT_USED
XHIF_D21	GPIO_*_2.21	NOT_USED	NOT_USED	NOT_USED
XHIF_D22	GPIO_*_2.22	NOT_USED	NOT_USED	NOT_USED
XHIF_D23	GPIO_*_2.23	NOT_USED	NOT_USED	NOT_USED
XHIF_D24	GPIO_*_2.24	NOT_USED	NOT_USED	NOT_USED
XHIF_D25	GPIO_*_2.25	NOT_USED	NOT_USED	NOT_USED
XHIF_D26	GPIO_*_2.26	NOT_USED	NOT_USED	NOT_USED
XHIF_D27	GPIO_*_2.27	NOT_USED	NOT_USED	NOT_USED
XHIF_D28	GPIO_*_2.28	NOT_USED	NOT_USED	NOT_USED
XHIF_D29	GPIO_*_2.29	NOT_USED	NOT_USED	NOT_USED

GPIO Pin	GPIO Registers	GPIO Alternative Function A	GPIO Alternative Function B	GPIO Alternative Function C
XHIF_D30	GPIO_*_2.30	NOT_USED	NOT_USED	NOT_USED
XHIF_D31	GPIO_*_2.31	NOT_USED	NOT_USED	NOT_USED

Table 24: GPIO Port 2 Input Mapping

7.6 Configuration Pins

To switch the ERTEC 200P between global use cases or several test-modes there are 7 EMC-Pins used as configuration pins. During active PowerOn-Reset XRESET the value of the inputs is latched in the SCR-B-Register CONFIG. After Reset the pins are operating according their function.

CONFIG (6) PIN: A23	CONFIG (5) PIN: A22	CONFIG (4) PIN: A21	CONFIG (3) PIN: A20	CONFIG (2) PIN: A19	CONFIG (1) PIN: A18	CONFIG (0) PIN: A17	Description
-	-	-	-	-	-	1	REF_CLK tristate
-	-	-	-	-	-	0	REF_CLK output (25 MHz)
-	-	-	-	-	0	-	ARM-Clock 125 MHz
-	-	-	-	-	1	-	ARM-Clock 250 MHz
-	-	-	-	0	-	-	CONFIG (2) must be tied to zero
0	0	-	0	-	-	-	XHIF = on, 16 bit Mode, GPIO94-79 and GPIO61-60 on (all inputs), XHIF_XWR has Read/Write-Control
0	0	-	1	-	-	-	XHIF = on, 16 bit Mode, GPIO94-79 and GPIO 61-60 on (all inputs), XHIF_XRD / XHIF_XWR separated
0	0	0	-	-	-	-	XHIF = on, 16 bit Mode, GPIO94-79 and GPIO 61-60 on (all inputs), XHIF_XRDY is high-active
0	0	1	-	-	-	-	XHIF = on, 16 bit Mode, GPIO94-79 and GPIO61-60 on (all inputs), XHIF_XRDY is low-active
0	1	-	0	-	-	-	XHIF = on, 32 bit mode, GPIO95-32 off, XHIF_XWR has Read/Write-Control
0	1	-	1	-	-	-	XHIF = on, 32 bit mode, GPIO95-32 off, XHIF_XRD / XHIF_XWR separated
0	1	0	-	-	-	-	XHIF = on, 32 bit mode, GPIO95-32 off, XHIF_XRDY is high-active
0	1	1	-	-	-	-	XHIF = on, 32 bit mode, GPIO95-32 off, XHIF_XRDY is low-active
1	0	0	1	-	-	-	XHIF = off, GPIO95-32 on (all inputs)
1	1	1	0	-	-	-	XHIF = off, ARM926 Trace Port = on (only at ARM926 Clock = 125 MHz)
Remainder				-	-	-	reserved

Blue: Default setting through the internal pulls

Table 25: Configuration Pins

A detailed mapping of the pins for each configuration can be found in /1/

7.7 Boot Pins

For the selection of the bootmodi 4 pins of the EMC-Interface are used. These Pins are latched in the SCR-B-Register BOOT_REG during PowerOn-Reset XRESET is active. The Pins operate in normal mode when XRESET is released.

BOOT(3) PIN: A16	BOOT(2) PIN: A15	BOOT(1) PIN: XOE_D	BOOT(0) PIN: DTXR	Boot from
X	X	X	X	all others -> reserved

1	0	0	0	Externes NOR-Flash (8 Bit) *)
1	0	0	1	Externes NOR- Flash (16 Bit) *)
1	1	0	1	SPI-Master Readcommand 0xe8
1	1	1	0	SPI-Master Readcommand 0x03
1	1	1	1	Hostinterface (XHIF)

*) the secondary bootloader in the boot-ram is not used

Table 26: Boot Pins

7.7.1 StartUp-Times

The ERTEC 200P needs the following StartUp-Times depending on the boot-modus:

<i>Boot from...</i>	t_1		t_2
NOR-Flash (8 Bit)	1,3 ms	1 Byte:	712ns
NOR- Flash (16 Bit)	1,3 ms	1 Halfword:	712ns
SPI-Master Readcommand 0xe8	1,1 ms	1 Byte :	14,7µs
SPI-Master Readcommand 0x03	1,1 ms	1 Byte :	14,7µs
Hostinterface (XHIF)	1,1 ms	depending on: - the accesstime of the ext. Masters - the configuration of the XHIF - the target memory (typ. ARM926 D-TCM)	

Table 27: StartUp-Times

t_1 : Time between release of RESET_N and loading the first data-byte of the 2nd bootloader.

Hint: The PLL-Setup-Time with 1035 µs is included in this time.

Additional Setup-Times depending on the Storage-Device are also included.

t_2 : access time for loading the 2nd bootloader

The StartUp-Time of the ERTEC 200P is therefore calculated as:

$$t_1 + (t_2 \times \text{number of user data 2nd Boot})$$

8 Thermal Specification

ERTEC 200P is intended for use in the operating ambient temperature range -40°C .. +85°C

Unit :deg. / W

Layer (PCB)	Ambient Temperature	Air Flow unit [m/s]				
		0	0.2	1	2	
6	25 deg	θ_{ja}	26.4	23.4	20.0	18.0
		Ψ_{jt}	0.14	0.17	0.24	0.29
		θ_{jc}	7.1			
		θ_{jb}	11.9			
6	85 deg	θ_{ja}	23.5	21.7	19.5	17.8
		Ψ_{jt}	0.2	0.2	0.3	0.3
		θ_{jc}	7.2			
		θ_{jb}	12.1			
8	25 deg	θ_{ja}	23.6	21.7	17.7	15.9
		Ψ_{jt}	0.14	0.16	0.22	0.26
		θ_{jc}	7.1			
		θ_{jb}	10.3			
8	85 deg	θ_{ja}	21.1	19.9	17.2	15.7
		Ψ_{jt}	0.16	0.17	0.23	0.27
		θ_{jc}	7.2			
		θ_{jb}	10.4			

Note : each value is estimated one

Condition
PCB(Layer6) : Layer construction by Siemens
PCB(Layer8) : Layer construction by Siemens
PKG : 400pinFPBGA

EIA/JEDEC51-1, 51-2 define thermal characters as follows,

θ_{ja} Thermal resistance, junction-to-ambient

Ψ_{jt} Thermal characterization parameter, junction to the top center of the package surface.

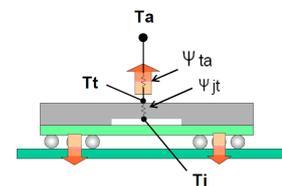
θ_{jc} Thermal resistance, junction-to-case

θ_{jb} Thermal resistance, junction-to-ball

$$T_i = T_a + \theta_{ja} \times P$$

$$T_t = T_i - \Psi_{jt} \times P$$

no use of external heat sinks



Example:

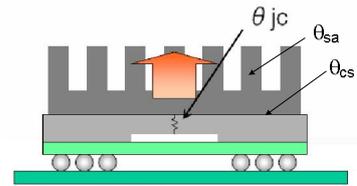
With $P = 1.52W$, $T_a = 85^\circ C$, 6 Layer PCB and no Air Flow T_j results in
 $T_j = 85^\circ C + 23.5^\circ C/W \times 1.52 W = 120.7^\circ C$

The Temperature on the top center of the Package surface results in
 $T_t = 123.1^\circ C - (0.2^\circ C/W \times 1.52 W) = 120.4^\circ C$

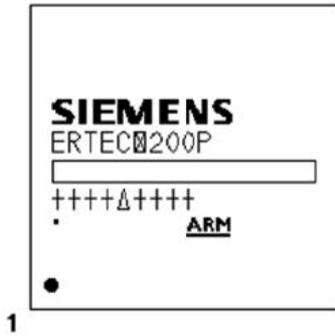
With the use of a heat sink

θ_{jc} Thermal resistance, junction-to-case
 θ_{cs} Thermal resistance, case-to-heat-sink
 θ_{sa} Thermal resistance, heat-sink-to-ambient

$$T_J = T_a + (\theta_{jc} + \theta_{cs} + \theta_{sa}) \times P$$



9 Package Information



Packaging = System in Package - Fine Pitch Ball Grid Array (SIP-FPBGA)
 Pitch = 0.8 mm
 Body-Size = 17 mm x 17 mm

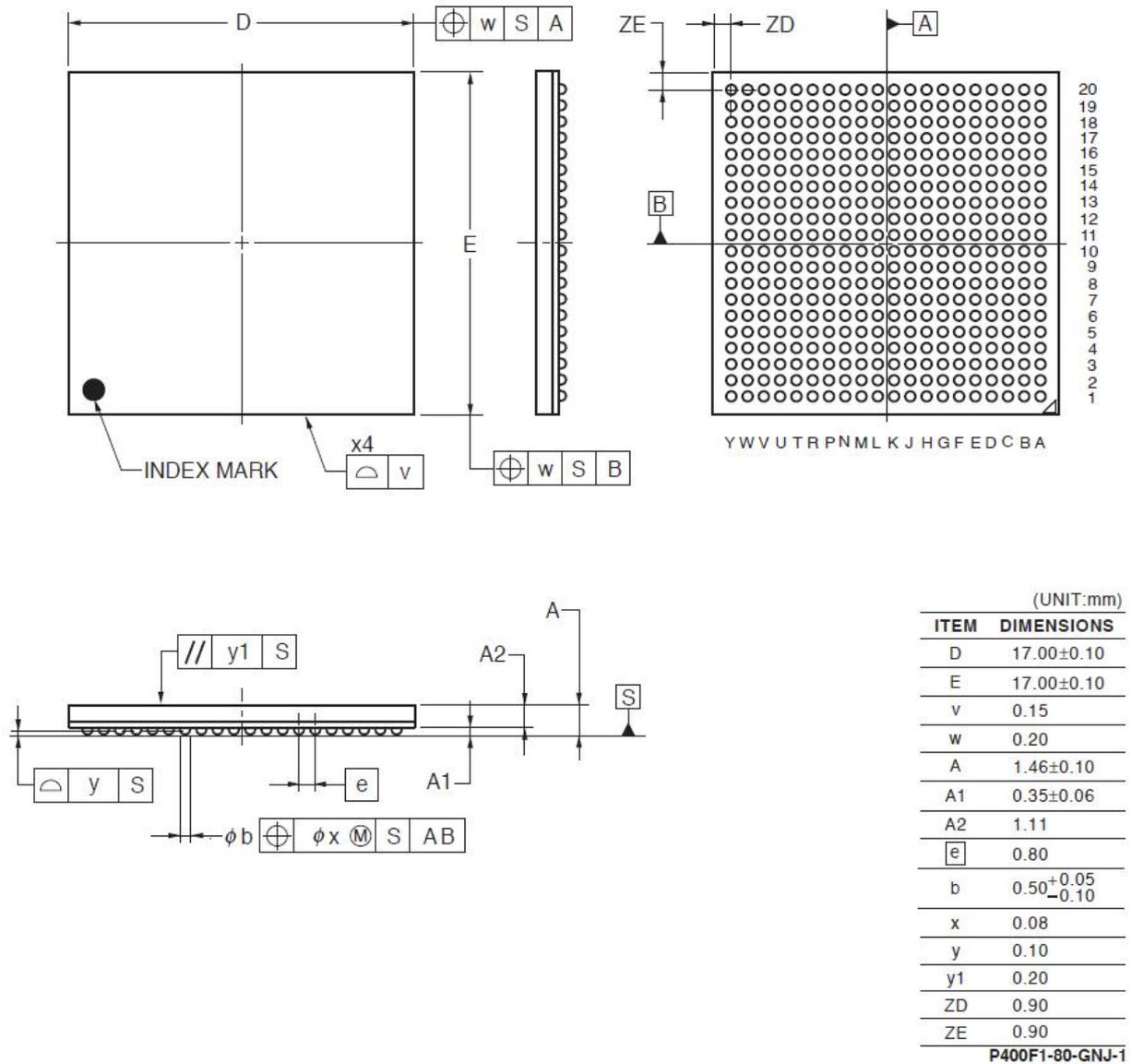
9.1 Ordering Info / Part Numbers

The Part-Number of the ERTEC 200P:

ERTEC 200P, 10 pcs: 6ES7195-0BH00-0XA0
 ERTEC 200P, 90 pcs: 6ES7195-0BH10-0XA0
 ERTEC 200P, 450 pcs: 6ES7195-0BH20-0XA0

9.2 400-Pin SIP-FPBGA Package

400-PIN PLASTIC FBGA (17x17)



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Figure 28: Package Information

9.3 Soldering Conditions

Solder this product ERTEC 200P (lead free device) under the following recommended conditions:

Soldering Method	Soldering Condition	Symbol of Recommended Soldering Condition
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (220°C min.), Number of times: 3 max., Number of days: 7 (see Note)	IR60-107-3

Note:

The number of days refers to storage at 25°C, 65% RH MAX after the dry pack has been opened.

After that, prebaking is necessary at 125 °C for 10 to 72 hours.

For details of the recommended soldering conditions, refer to the information document:

Renesas Semiconductor Package Mount Manual

9.4 Packing Information

max 90 pices are packed into one tray.

The dimensions of a tray are:

135,9mm x 322,6mm x 7,62 mm

max. 5 trays are packed into an inner box.

The dimensions of an inner box are:

175mm x 375mm x 75 mm

9.5 Ballout

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Y	Y20(39) VDD33	Y19(38) GND	Y18(37) GPIO28	Y17(36) GPIO29	Y16(35) VDD33	Y15(34) GND	Y14(33) CLKP_A	Y13(32) GND	Y12(31) P2RDXN	Y11(30) P2SDXN	Y10(29) GND	Y9(28) P2TDXN	Y8(27) P2FXEN	Y7(26) VDD33	Y6(25) GND	Y5(24) VDD_EMC	Y4(23) D0	Y3(22) D15	Y2(21) GND	Y1(20) VDD_EMC
W	W20(40) GND	W19(111) GPIO24	W18(110) GPIO25	W17(109) GPIO26	W16(108) REF_CLK	W15(107) XRESET	W14(106) CLKP_B	W13(105) VDD33	W12(104) P2RDXP	W11(103) P2SDXP	W10(102) GPIO0	W9(101) P2TDXP	W8(100) TDI	W7(99) RTCK	W6(98) GND	W5(97) VDD_EMC	W4(96) D3	W3(95) D13	W2(94) D11	W1(19) GND
V	V20(41) GPIO27	V19(112) GPIO30	V18(175) GPIO31	V17(174) GPIO15_IN	V16(173) GND	V15(172) AVDD	V14(171) AGND	V13(170) VDD15	V12(169) GND	V11(168) VDD15	V10(167) TESTDOUT7	V9(166) GPIO0_INT	V8(165) GND	V7(164) VDD15	V6(163) D2	V5(162) D2	V4(161) D1	V3(160) D14	V2(93) D9	V1(18) D12
U	U20(42) L_PHY_1	U19(113) L_PHY_2	U18(176) GPIO14_IN	U17(231) GPIO13_IN	U16(230) GPIO23	U15(229) GPIO21	U14(228) GPIO20	U13(227) GPIO7_INT	U12(226) GPIO6_INT	U11(225) GPIO5_INT	U10(224) GPIO4_INT	U9(223) GPIO3_INT	U8(222) GPIO2_INT	U7(221) GPIO1_INT	U6(220) DTXR	U5(219) D7	U4(218) D5	U3(159) D6	U2(92) D8	U1(17) D10
T	T20(43) GND	T19(114) VDD33	T18(177) GPIO12_IN	T17(232) GPIO11_IN	T16(279) GPIO19	T15(278) GPIO18	T14(277) A_PHY_1	T13(276) A_PHY_2	T12(275) RYP_CLK	T11(274) GPIO17	T10(273) GPIO16	T9(272) TMS	T8(271) TAP_SEL	T7(270) KOE_DRIVER	T6(269) XBE2_DGM2	T5(268) XCS_PER0	T4(217) XBE1_DGM1	T3(158) VDD_EMC	T2(91) VDD_EMC	T1(16) VDD_EMC
R	R20(44) D_VDD3	R19(115) D_GND3	R18(178) GPIO22	R17(233) GPIO8_INT	R16(280) GND	R15(319) TMC2	R14(318) VDD33	R13(317) TACT	R12(316) GND	R11(315) XSRST	R10(314) TEST	R9(313) VDD33	R8(312) TDO	R7(311) GND	R6(310) XCS_PER1	R5(267) A23	R4(216) A22	R3(157) GND	R2(90) GND	R1(15) GND
P	P20(45) P2VDDARXTX	P19(116) VDD15	P18(179) GND	P17(234) XHIF_D1	P16(281) XHIF_D15	P15(320) VDD33	P14(351) GND	P13(350) VDD33	P12(349) GND	P11(348) VDD12	P10(347) VDD12	P9(346) GND	P8(345) VDD33	P7(344) GND	P6(309) NC	P5(266) A21	P4(215) MTAST	P3(156) TCK	P2(89) A20	P1(14) A19
N	N20(46) P2RXN	N19(117) P2RXP	N18(180) PVSSA	N17(235) XHIF_D10	N16(282) XHIF_D13	N15(321) VDD_XHIF	N14(352) VDD_XHIF	N13(375) GND	N12(374) GND	N11(373) VDD12	N10(372) VDD12	N9(371) GND	N8(370) VDD_EMC	N7(343) VDD_EMC	N6(308) CLK_O_BE	N5(265) A18	N4(214) VDD15	N3(155) A17	N2(88) XWR	N1(13) M1(12)
M	M20(47) P2TXN	M19(118) P2TXP	M18(181) PVSSA	M17(236) XHIF_D9	M16(283) XHIF_D6	M15(322) CTRL_STBY1	M14(353) GND	M13(376) GND	M12(391) GND	M11(390) GND	M10(389) GND	M9(388) GND	M8(369) GND	M7(342) GND	M6(307) CLK_O_BE	M5(264) A15	M4(213) VDD33	M3(154) A16	M2(87) A16	M1(12) XRD
L	L20(48) VDDACR	L19(119) VSSA	L18(182) GND	L17(237) XHIF_D4	L16(284) XHIF_D5	L15(323) XHIF_XRDY	L14(354) VDD12	L13(377) VDD12	L12(392) GND	L11(399) GND	L10(398) GND	L9(387) GND	L8(368) VDD12	L7(341) VDD12	L6(306) GND	L5(263) CLK_L_BE	L4(212) XRDY_BE	L3(153) GND	L2(86) A14	L1(11) GND
K	K20(49) VDDAPLL	K19(120) EXTRES	K18(183) ATP	K17(238) XHIF_D8	K16(285) XHIF_D7	K15(324) GND	K14(355) VDD12	K13(378) VDD12	K12(393) GND	K11(400) GND	K10(397) GND	K9(386) GND	K8(367) VDD12	K7(340) VDD12	K6(305) VDD33	K5(262) XAV_BE	K4(211) XWE_SDRAM	K3(152) XCS_SDRAM	K2(85) A13	K1(10) VDD_EMC
J	J20(50) P1TXN	J19(121) P1TXP	J18(184) PVSSA	J17(239) XHIF_D14	J16(286) XHIF_D11	J15(325) CTRL_STBY1	J14(356) GND	J13(379) GND	J12(394) GND	J11(395) GND	J10(396) GND	J9(385) GND	J8(366) GND	J7(339) GND	J6(304) CLK_O_SDRAM	J5(261) CLK_O_SDRAM	J4(210) XRS_SDRAM	J3(151) XCS_SDRAM	J2(84) A11	J1(9) A12
H	H20(51) P1RXN	H19(122) P1RXP	H18(185) PVSSA	H17(240) XHIF_D4	H16(287) XHIF_D12	H15(326) VDD_XHIF	H14(357) VDD_XHIF	H13(380) GND	H12(381) GND	H11(382) VDD12	H10(383) VDD12	H9(384) GND	H8(365) GND	H7(338) VDD_EMC	H6(303) VDD_EMC	H5(260) CLK_O_SDRAM	H4(209) A0	H3(150) GND	H2(83) A10	H1(8) A9
G	G20(52) P1VDDARXTX	G19(123) VDD15	G18(186) VDD33ESD	G17(241) XHIF_D0	G16(288) XHIF_D3	G15(327) XHIF_XIRD	G14(358) GND	G13(359) VDD_XHIF	G12(360) GND	G11(361) VDD12	G10(362) VDD12	G9(363) GND	G8(364) VDD_XHIF	G7(337) GND	G6(302) XRDY_BE	G5(259) CLK_L_SDRAM	G4(208) A1	G3(149) VDD33	G2(82) A7	G1(7) A6
F	F20(53) E20(54)	F19(124) E19(125)	F18(187) E18(188)	F17(242) E17(243)	F16(289) E16(290)	F15(328) E15(291)	F14(329) E14(292)	F13(330) E13(293)	F12(331) E12(294)	F11(332) E11(295)	F10(333) E10(296)	F9(334) E9(297)	F8(335) E8(298)	F7(336) E7(299)	F6(301) E6(300)	F5(258) E5(257)	F4(207) E4(206)	F3(148) E3(147)	F2(81) E2(80)	F1(6) E1(5)
E	D20(55) XHIF_XWR	D19(126) XHIF_A19	D18(189) XHIF_SEG_1	D17(244) XHIF_A15	D16(245) XHIF_SEG_2	D15(246) XHIF_A5	D14(247) XHIF_D28	D13(248) XHIF_D26	D12(249) XHIF_D29	D11(250) XHIF_D22	D10(251) XHIF_D24	D9(252) XHIF_D23	D8(253) XHIF_D20	D7(254) XHIF_D19	D6(255) XCS_PER2	D5(256) XBE2_DGM2	D4(205) D18	D3(146) XBE1_DGM3	D2(79) D31	D1(4) D29
D	C20(56) XHIF_XRD	C19(127) XHIF_A12	C18(190) XHIF_A11	C17(191) XHIF_A6	C16(192) XHIF_A16	C15(193) XHIF_A2	C14(194) XHIF_A14	C13(195) VDD33	C12(196) GND	C11(197) VDD15	C10(198) VDD15	C9(199) P1FXEN	C8(200) VDD33	C7(201) GND	C6(202) VDD15	C5(203) D20	C4(204) D17	C3(145) D30	C2(78) D27	C1(3) D28
C	B20(57) GND	B19(128) XHIF_A10	B18(129) XHIF_A8	B17(130) XHIF_A3	B16(131) XHIF_A13	B15(132) XHIF_A8	B14(133) XHIF_A8	B13(134) GND	B12(135) P1RDXP	B11(136) P1SDXP	B10(137) GPIO0	B9(138) P1TDXP	B8(139) TESTDOUT5	B7(140) GND	B6(141) VDD_EMC	B5(142) D19	B4(143) D22	B3(144) D25	B2(77) D26	B1(2) GND
B	A20(58) VDD_XHIF	A19(59) GND	A18(60) VDD_XHIF	A17(61) XHIF_XCS_M	A16(62) XHIF_A1	A15(63) XHIF_A17	A14(64) VDD_XHIF	A13(65) GND	A12(66) P1RDXN	A11(67) P1SDXN	A10(68) GND	A9(69) P1TDXN	A8(70) TESTDOUT6	A7(71) GND	A6(72) VDD_EMC	A5(73) D21	A4(74) D23	A3(75) D24	A2(76) GND	A1(1) VDD_EMC

Figure 29: Ballout ERTEC 200P

10 Quality Information

10.1 Life time / (HW) FIT-Rate

Junction-Temperature	125 °C
ERTEC 200P Complete	315

Conditions:

Ea=0.7eV, C.L=60%, 24h/10yrs

11 Literature / References

- /1/ ERTEC200P_Manual_en.pdf
- /2/ ETM9 Technical Reference Manual (Rev. 2a) (ARM DDI 0157E)