S7-400 Instruction List

CPU 412, 414, 416, 417

This Instruction List has the order number:

6ES7498-8AA05-8BN0

and is part of the documentation package with the order number **6ES7498-8AA05-8BA0**

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Disclaimer of Liability

We have checked the contents of this manual for agreement with the hardware and software described. Since deviations cannot be precluded entirely, we cannot guarantee full agreement. However, the data in this manual are reviewed regularly and any necessary corrections included in subsequent editions. Suggestions for improvement are welcomed.

Siemens Aktiengesellschaft

6ES7498-8AA05-8BN0

Contents

Applicability

This list of instructions applies to the CPUs listed below.

Name	Order number	subsequently described as[1)]
CPU 412-1	6ES7412-1XJ05-0AB0	CPU 412
CPU 412-2	6ES7412-2XJ05-0AB0	
CPU 414-2	6ES7414-2XK05-0AB0	CPU 414
CPU 414-3	6ES7414-3XM05-0AB0	
CPU 414-3 PN/DP	6ES7414-3EM05-0AB0	
CPU 416-2	6ES7416-2XN05-0AB0	CPU 416
CPU 416F-2	6ES7416-2FN05-0AB0	
CPU 416-3	6ES7416-3XR05-0AB0	
CPU 416-3 PN/DP	6ES7416-3ER05-0AB0	
CPU 416F-3 PN/DP	6ES7416-3FR05-0AB0	
CPU 417-4	6ES7417-4XT05-0AB0	CPU 417

1) except in the tables, where a detailed differentiation is necessary

Address Identifier and Parameter Ranges

Addr. ID	Parameter Range				Description
	CPU 412	CPU 414	CPU 416	CPU 417	
Q[1)]	0.0 to 127.7	0.0 to 255.7	0.0 to 511.7	0.0 to 1023.7	Output (in PIQ)
QB[1)]	0 to 127	0 to 255	0 to 511	0 to 1023	Output byte (in PIQ)
QW[1)]	0 to 126	0 to 254	0 to 510	0 to 1022	Output word (in PIQ)
QD[1)]	0 to 124	0 to 252	0 to 508	0 to 1020	Output double word (in PIQ)
DBX	0.0 to 65533.7				Data bit in data block
DB	1 to 16000[2)]				Data block
DBB	0 to 65533				Data byte in DB
DBW	0 to 65532				Data word in DB
DBD	0 to 65530				Data double word in DB
DIX	0.0 to 65533.7				Data bit in instance DB
DI	1 to 16000[2)]				Instance data block
DIB	0 to 65533				Data byte in instance DB
DIW	0 to 65532				Data word in instance DB
DID	0 to 65530				Data double word instance DB

1) Default setting can be changed, see Technical Specifications in the manual *CPU Specifications*

2) Number of DBs for CPU 412-1: 1500, number of DBs for CPU 412-2: 3000, number of DBs for CPU 414: 6000, number of DBs for CPU 416: 10000, number of DBs for CPU 417: 16000

Address Identifier and Parameter Ranges, continued

Addr. ID	Parameter Range				Description
	CPU 412	CPU 414	CPU 416	CPU 417	
I[1)]	0.0 to 127.7	0.0 to 255.7	0.0 to 511.7	0.0 to 1023.7	Input bit (in PII)
IB[1)]	0 to 127	0 to 255	0 to 511	0 to 1023	Input byte (in PII)
IW[1)]	0 to 126	0 to 254	0 to 510	0 to 1022	Input word (in PII)
ID[1)]	0 to 124	0 to 252	0 to 508	0 to 1020	Input double word (in PII)
L[1)]	0.0 to 4095.7	0.0 to 8191.7	0.0 to 16383.7	0.0 to 32767.7	Local data
LB[1)]	0 to 4095	0 to 8191	0 to 16383	0 to 32767	Local data byte
LW[1)]	0 to 4094	0 to 8190	0 to 16382	0 to 32766	Local data word
LD[1)]	0 to 4092	0 to 8188	0 to 16380	0 to 32764	Local data double word
M	0.0 to 4095.7	0.0 to 8191.7	0.0 to 16383.7	0.0 to 16383.7	Bit memory
MB	0 to 4095	0 to 8191	0 to 16383	0 to 16383	memory byte
MW	0 to 4094	0 to 8190	0 to 16382	0 to 16382	memory word
MD	0 to 4092	0 to 8188	0 to 16380	0 to 16380	memory double word

1) Default setting can be changed, see Technical Specifications in the manual *CPU Specifications*

Address Identifier and Parameter Ranges, continued

Addr. ID	Parameter Range				Description
	CPU 412	CPU 414	CPU 416	CPU 417	
PQB	0 to 4095	0 to 8191	0 to 16383	0 to 16383	Peripheral output byte (direct I/O access)
PQW	0 to 4094	0 to 8190	0 to 16382	0 to 16382	Peripheral output word (direct I/O access)
PQD	0 to 4092	0 to 8188	0 to 16380	0 to 16380	Peripheral output double word (direct I/O access)
PIB	0 to 4095	0 to 8191	0 to 16383	0 to 16383	Peripheral input byte (direct I/O access)
PIW	0 to 4094	0 to 8190	0 to 16382	0 to 16382	Peripheral input word (direct I/O access)
PID	0 to 4092	0 to 8188	0 to 16380	0 to 16380	Peripheral output double word (direct I/O access)
T	0 to 2047	0 to 2047	0 to 2047	0 to 2047	Timer
C	0 to 2047	0 to 2047	0 to 2047	0 to 2047	Counter

Constants and Ranges

Constant	Range	Description
B(b1,b2) B(b1,b2,b3,b4)	–	Constant, 2 or 4 bytes
D# Date	–	IEC date constant
L# Integer	–	32-bit integer constant
P# Bit pointer	–	Pointer constant
S5T# Time value	–	S7 time constant [1]
T# TIme value	—	Time constant
TOD# Time value	–	IEC time constant
C# Count value	–	Counter constant (BCD code)
2#n	–	Binary constant
W#16# DW#16#	–	Hexadecimal constant

1) For loading of S7 timers.

Abbreviations and Mnemonics

The following abbreviations and mnemonics are used in the Instruction List:

Abbrev.	Description	Example
k8	8-bit constant 0 to 255	32
k16	16-bit constant 256 to 32 767	28 131
k32	32-bit constant 32 768 to 999 999 999	127 624
i8	8-bit integer -128 to +127	-113
i16	16-bit integer -32768 to +32767	+6523
i32	32-bit integer -2 147 483 648 to +2 147 483 647	-2 222 222
m	Pointer constant	P#240.3
n	Binary constant	1001 1100
p	Hexadecimal constant	EA12
Label	Symbolic jump address (max. 4 characters)	DESTINATION
a	Byte address	

Abbreviations and Mnemonics, continued

Abbrev.	Description	Example
b	Bit address	
c	Address area	I, Q, M, L, DBX, DIX
d	Address in: MD, DBD, DID or LD	
e	Number in: MW, DBW, DIW or LW	
f	Timer/counter No.	
g	Address area	IB, QB, PIB, PQB, MB, LB, DBB, DIB
h	Address area	IW, QW, PIW, PQW, MW, LW, DBW, DIW
i	Address area	ID, QD, PID, PQD, MD, LD, DBD, DID
q	Block No.	

Registers

ACCU1 to ACCU4 (32 Bits)

The accumulators are registers for processing bytes, words or double words. The address identifiers are loaded into the accumulators, where they are logically gated. The result of the logic operation (RLO) is in ACCU1 and can be transferred from there to a memory cell.

The accumulators are 32 bits long.

Accumulator designations :

ACCU	Bits
ACCUx (x = 1 to 4)	Bit 0 to 31
ACCUx-L	Bit 0 to 15
ACCUx-H	Bit 16 to 31
ACCUx-LL	Bit 0 to 7
ACCUx-LH	Bit 8 to 15
ACCUx-HL	Bit 16 to 23
ACCUx-HH	Bit 24 to 31

Address Registers AR1 and AR2 (32 Bits)

The address registers contain the area-internal or area-crossing pointers for instructions using indirect addressing. The address registers are 32 bits long.

The area-internal and/or area-crossing pointers have the following syntax:

- Area-internal pointer `00000000 00000bbb bbbbbbbb bbbbbxxx`
- Area-crossing pointer **`yyyyyyyy`** `00000bbb bbbbbbbb bbbbbxxx`

Legend:

`b`	Byte address
`x`	Bit number
`y`	Area identifier (see “Examples of Addressing”)

Status Word (16 Bits)

The status word bits are evaluated or set by the instructions.

The status word is 16 bits long.

Bit	Assignment	Description
0	/FC	First check bit
1	RLO	Result of logic operation
2	STA	Status
3	OR	Or (AND before OR)
4	OS	Stored overflow
5	OV	Overflow
6	CC 0	Condition code 0
7	CC 1	Condition code 1
8	BR	Binary result
9 to 15	Unassigned	–

Examples of Addressing

Addressing Examples	Description
Immediate Addressing	
L +27	Load 16-bit integer constant “27” into ACCU1
L L#-1	Load 32-bit integer constant “-1” into ACCU1
L 2#1010101010101010	Load binary constant into ACCU1
L DW#16#A0F0BCFD	Load hexadecimal constant into ACCU1
L ’ENDE’	Load ASCII character into ACCU1
L T#500 ms	Load time value into ACCU1
L C#100	Load count value into ACCU1
L B#(100,12)	Load 2-byte constant
L B#(100,12,50,8)	Load 4-byte constant
L P#10.0	Load area-internal pointer into ACCU1
L P#E20.6	Load area-crossing pointer into ACCU1
L -2.5	Load real number into ACCU1
L D# 1995-01-20	Load date
L TOD 13:20:33.125	Load time of day

Addressing Examples	Description
Direct Addressing	
A I 0.0	ANDing of input bit 0.0
L IB 1	Load input byte 1 into ACCU1
L IW 0	Load input word 0 into ACCU1
L ID 0	Load input double word 0 into ACCU1
Indirect Addressing of Timers/Counters	
SP T [LW 8]	Start timer; the timer number is in local data word 8
CU C [LW 10]	Count upwards; the counter number is in local data word 10
Area-Internal Memory-Indirect Addressing	
A I [LD 12] Example: L P#22.2 T LD 12 A I [LD 12]	AND operation: The address of the input is in local data double word 12 as pointer
A I [DBD 1]	AND operation: The address of the input is in data double word 1 of the open DB as pointer
A I [DID 12]	AND operation: The address of the output is in data double word 12 of the open instance DB as pointer
A I [MD 12]	AND operation: The address of the output is in memory double word 12 as pointer

Examples of Addressing, continued

Addressing Examples
Area-Internal Register-Indirect Addressing
A I [AR1,P#12.2]
Area-Crossing Register-Indirect Addressing

For area-crossing register-indirect addressing, the address must also contain an area identifier. The address is in the address register. The area identifiers are as follows:

Area identifier	Coding (binary)	hex.	Area
P	1000 0**000**	80	I/O area
I	1000 0**001**	81	Input area
Q	1000 0**010**	82	Output area
M	1000 0**011**	83	Bit memory area
DB	1000 0**100**	84	Data area
DI	1000 0**101**	85	Instance data area
L	1000 0**110**	86	Local data area
VL	1000 0**111**	87	Predecessor local data area (access to local data of invoking block)

L B [AR1,P#8.0]	Load byte into ACCU1: The address is calculated from the “pointer value in AR 1 + P#8.0”
A [AR1,P#32.3]	AND operation: The address of the operand is calculated from the “pointer value in AR 1 + P#32.3”
Addressing Via Parameters	
A Parameter	Addressing via parameters

Examples of how to calculate the pointer

- **Example for sum of bit addresses $\leq$7:**

  LAR1 P#8.2
  A I [AR1,P#10.2]

Result: Input 18.4 is addressed (by adding the byte and bit addresses)

- **Example for sum of bit addresses>7:**

  L P#10.5
  LAR1
  A I [AR1,P#10.7]

Result: Input 21.4 is addressed (by adding the byte and bit addresses with carry over)

Execution Times with Indirect Addressing

When using indirect addresses statement consists of two parts:

Part 1: Load the address of the instruction

Part 2: Execute the instruction

In other words, when working with indirect addresses, you must calculate the execution time of an instruction from these two parts.

Calculating the Execution Time

The total execution time is calculated as follows:

	Time required for loading the address
+	execution time of the instruction
=	Total execution time of the instruction

The execution times listed in the chapter entitled “List of Instructions” apply to the execution times of the second part of an instruction, i.e. for the actual execution of an instruction.

You must then add the time required for loading the address of the instruction to this execution time (see following Table).

The execution time for loading the address of the instruction from the various areas is shown in the following table.

Address is in ...	Execution Time in ns			
	CPU 412	**CPU 414**	**CPU 416**	**CPU 417**
Bit memory area M Word Double word	 150 150	 90 90	 60 60	 36 36
Data block DB/DX Word Double word	 175 175	 105 105	 70 70	 42 42
Local data area L Word Double word	 150 150	 90 90	 60 60	 36 36
AR1/AR2 (area-internal)	0 [1]	0 [1]	0 [1]	0 [1]
AR1/AR2 (area-crossing)	0 [1]	0 [1]	0 [1]	0 [1]
Parameter (word) ... for: • Timers • Counters • Block calls	 175 175 175	 105 105 105	 70 70 70	 42 42 42
Parameter (double word) ... for Bits, bytes, words and double words	175	105	70	42

[1] Address registers AR1/AR2 do not need to be loaded in separate cycles for addressing.

The pages that follow contain examples for calculating the instruction run time for the various indirectly addressed instructions.

Examples of Calculations

You will find a few examples here for calculating the execution times for the various methods of indirect addressing.

Calculating the Execution Times for Area-Internal Memory-Indirect Addressing

Example: A I [DBD 12] with CPU 414

Step 1: Load the contents of DBD 12 (time required is listed in the table on page 20)

Address is in ...	Execution Time in ns
Bit memory area M Word Double word	 90 90
Data block DB/DX Word Double word	 105 105

Step 2: AND the input addressed in this way (you will find the execution time in the tables in the chapter entitled “List of Instructions” on page 23)

Typical Execution Time in ns	
Direct Addressing	**Indirect Addressing**
45 :	Time for A I **45+** **:**

Total execution time:

105 ns
\+ 45 ns
150 ns

Execution Time for Area-Crossing Register-Indirect Addressing

Example: A [AR1, P#23.1] ... with I 1.0 in AR1 with CPU 416

Step 1: Load the contents of AR1, and increment them by the offset 23.1 (the time required is in the table on page 20)

Address is in ...	Execution Time in ns
:	:
AR1/AR2 (area-crossing)	0
:	:

Step 2: AND link of the input addressed this way (see page 24 for the execution time)

Typical Execution Time in ns	
Direct Addressing	**Indirect Addressing**
30	Time for A I **30+**
:	**:**

Total execution time:

0ns
+ 30ns
30ns

List of Instructions

This chapter contains the complete list of instructions for the S7-400 CPUs. The descriptions have been kept as concise as possible. You will find a detailed functional description in the various STEP 7 reference manuals.
Please note that, in the case of indirect addressing (examples see page 16), you must add the time required for loading the address of the particular instruction to the execution times listed (see page 19).

Bit Logic Instructions

All logic instructions generate a result (new RLO). The first instruction in a logic string generates the new RLO from the signal state scanned. The subsequent logic instructions generate the new RLO from the signal state scanned and the old RLO. The logic string ends with an instruction which limits the RLO (e.g. a memory instruction); that is, the /FC bit is set to zero.

Instr.	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
A/AN							
	I/Q a.b	Input/output	1[1]/2	75	45	30	18
	M a.b	Bit memory	1[2]/2	75	45	30	18
	L a.b	Local data bit	2	75	45	30	18
	DBX a.b	Data bit	2	100	60	40	24
	DIX a.b	Instance data bit	2	100	60	40	24
	c [d]	Memory-indirect, area-internal[3]	2	75+/100+	45+/60+	30+/40+	18+/24+
	c [AR1,m]	Register-ind., area-internal (AR1)[3]	2	75+/100+	45+/60+	30+/40+	18+/24+
	c [AR2,m]	Register-ind., area-internal (AR2)[3]	2	75+/100+	45+/60+	30+/40+	18+/24+
	[AR1,m]	Area-crossing (AR1)[3]	2	75+/100+	45+/60+	30+/40+	18+/24+
	[AR2,m]	Area-crossing (AR2)[3]	2	75+/100+	45+/60+	30+/40+	18+/24+
	Parameter	Via parameter [3]	2	75+/100+	45+/60+	30+/40+	18+/24+

Statusword for: **A/AN**	BIE	A1	A0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	–	–	–	–	–	Yes	–	Yes	Yes
Instruction affects:	–	–	–	–	–	Yes	Yes	Yes	1

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing;Address area 0 to 127
2) With direct instruction addressing;Address area 0 to 255
3) I,Q,M,L / DB, DI

Bit Logic Instructions, continued

Instr.	Address-ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
O/ON		OR/OR-NOT					
	I/Q a.b	Input/output	1[1)]/2	75	45	30	18
	M a.b	Bit memory	1[2)]/2	75	45	30	18
	L a.b	Local da	2	75	45	30	18
	DBX a.b	Data bit	2	100	60	40	24
	DIX a.b	Instance data bit	2	100	60	40	24
	c [d]	Memory-indirect, area-internal [3)]	2	75+/100+	45+/60+	30+/40+	18+/24+
	c [AR1,m]	Register-ind., area-internal (AR1) [3)]	2	75+/100+	45+/60+	30+/40+	18+/24+
	c [AR2,m]	Register-ind., area-internal (AR2) [3)]	2	75+/100+	45+/60+	30+/40+	18+/24+
	[AR1,m]	Area-crossing (AR1) [3)]	2	75+/100+	45+/60+	30+/40+	18+/24+
	[AR2,m]	Area-crossing (AR2) [3)]	2	75+/100+	45+/60+	30+/40+	18+/24+
	Parameter	Via parameter [3)]	2	75+/100+	45+/60+	30+/40+	18+/24+

Statusword for: **O, ON**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	Yes
Instruction affects:	–	–	–	–	–	0	Yes	Yes	1

\+ Plus time required for loading the address of the instruction (see page 20)

1) With direct instruction addressing; Address area 0 to 127

2) With direct instruction addressing; Address area 0 to 255

3) I,Q,M,L / DB, DI

Bit Logic Instructions, continued

Instr.	Address-ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
X/XN		EXKLUSIV-OR/ EXKLUSIV-OR-NOT					
	E/A a.b	Input/output	2	75	45	30	18
	M a.b	Bit memory	2	75	45	30	18
	L a.b	Local data bit	2	75	45	30	18
	DBX a.b	Data bit	2	100	60	40	24
	DIX a.b	Instance data bit	2	100	60	40	24
	c [d]	Memory-indirect, area-internal. 1)	2	75+/100+	45+/60+	30+/40+	18+/24+
	c [AR1,m]	Register-ind., area-internal (AR1) 1)	2	75+/100+	45+/60+	30+/40+	18+/24+
	c [AR2,m]	Register-ind., area-internal (AR2) 1)	2	75+/100+	45+/60+	30+/40+	18+/24+
	[AR1,m]	Area-crossing (AR1) 1)	2	75+/100+	45+/60+	30+/40+	18+/24+
	[AR2,m]	Area-crossing (AR2) 1)	2	75+/100+	45+/60+	30+/40+	18+/24+
	Parameter	Via parameter 1)	2	75+/100+	45+/60+	30+/40+	18+/24+

Status word for: **X, XN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	Yes
Instruction affects:	–	–	–	–	–	0	Yes	Yes	1

+Plus time required for loading the address of the instruction (see page 20)

1) I,Q,M,L / DB, DI

Bit Logic Instructions with Parenthetical Expressions

Saving the RLO and OR bits and the relevant function identifier (A, AN, ...) to the nesting stack. Seven nesting levels are possible per block. After the right parenthesis, the logic operation indicated by the function identifier is performed on the saved RLO and the current RLO; the current OR is overwritten with the saved OR.

In-struc-tion	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
A(		AND left parenthesis	1	75	45	30	18
AN(		AND NOT left parenthesis	1	75	45	30	18
O(		OR left parenthesis	1	75	45	30	18
ON(		OR NOT left parenthesis	1	75	45	30	18
X(		Exclusive OR left parenthesis	1	75	45	30	18
XN(		EXKLUSIV-ODER-NICHT-Klam-parenthesis	1	75	45	30	18

Statusword for: **A(, AN(, O(, ON(, X(, XN(**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	Yes	–	Yes	Yes
Instruction affects:	–	–	–	–	–	0	1	–	0

Bit Logic Instructions with Parenthetical Expressions, continued

In-struc-tion	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
)		Right parenthesis, removing an entry from the nesting stack.	1	75	45	30	18

Statusword for: **)**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	Yes	1	Yes	1

ORing of AND Instructions

The ORing of AND instructions is implemented according to the rule: AND before OR.

In-struc-tion	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
O		ORing of AND operations according to the rule: AND before OR	1	75	45	30	18

Status word for: **O**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	Yes
Instruction affects:	–	–	–	–	–	Yes	1	–	Yes

Logic Instructions with Timers and Counters

Examining the status of the addressed timer/counter and gating the result with the RLO according to the appropriate logic function.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
A/AN		AND/AND NOT					
	T f	Timer	1[1)]/2	75	45	30	18
	T [e]	Timer, memory-indirect addressing	2	75+	45+	30+	18+
	C f	Counter	1[1)]/2	75	45	30	18
	C [e]	Counter, memory-indirect addressing	2	75+	45+	30+	18+
	Timerpara. Counter para.	Timer/counter (addressing via parameter)	2	75+ 75+	45+ 45+	30+ 30+	18+ 18+

Status word for: **A, AN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	Yes	–	Yes	Yes
Instruction affects:	–	–	–	–	–	Yes	Yes	Yes	1

\+ Plus time required for loading the address of the instruction (see page 20)

1) With direct instruction addressing ;Address area 0 to 255

Logic Instructions with Timers and Counters, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
O/ON							
	T f	Timer	1[1)]/2	75	45	30	18
	T [e]	Timer, memory-indirect addr.	2	75+	45+	30+	18+
	C f	Counter	1[1)]/2	75	45	30	18
	C [e]	Counter, memory-indirect addressing	2	75+	45+	30+	18+
	Timerpara.	Timer/counter (addressing via parame-	2	75+	45+	30+	18+
	Counterpara.	ter)		75+	45+	30+	18+
X/XN		EXCLUSIVE OR/EXCLUSIVE OR NOT					
	T f	Timer	2	75	45	30	18
	T [e]	Timer, memory-indirect addr.	2	75+	45+	30+	18+
	C f	Counter	2	75	45	30	18
	C [e]	Counter, mem.-indirect addr.	2	75+	45+	30+	18+
	Timerpara.	EXCLUSIVE OR timer/counter (address-	2	75+	45+	30+	18+
	Counterpara.	ing via parameter)		75+	45+	30+	18+

Status word for: **O, ON, X, XN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	Yes
Instruction affects:	–	–	–	–	–	0	Yes	Yes	1

\+ Plus time required for loading the address of the instruction (see page 20)

1) With direct instruction addressing; address area 0 to 255

Word Logic Instructions with the Contents of Accumulator 1

Gating the contents of ACCU1 and/or ACCU1-L with a word or double word according to the appropriate function. The word or double word is either specified in the instruction as an address or is in ACCU2. The result is in ACCU1 and/or ACCU1-L.

In-struc-tion	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
AW		AND ACCU2-L	1	75	45	30	18
AW	W#16#p	AND 16-bit constant	2	75	45	30	18
OW		OR ACCU2-L	1	75	45	30	18
OW	W#16#p	OR 16-bit constant	2	75	45	30	18
XOW		EXCLUSIVE OR ACCU2-L	1	75	45	30	18
XOW	W#16#p	EXKLUSIV-ODER EXCLUSIVE OR 16-bit constant	2	75	45	30	18

Status word for: **AW, OW, XOW**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	ja	0	0	–	–	–	–	–

Word Logic Instructions with the Contents of Accumulator 1, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
AD		AND ACCU2	1	75	45	30	18
AD	DW#16#p	AND 32-bit constant	3	113	68	45	27
OD		OR ACCU2	1	75	45	30	18
OD	DW#16#p	OR 32-bit constant	3	113	68	45	27
XOD		EXCLUSIVE OR ACCU2	1	75	45	30	18
XOD	DW#16#p	EXCLUSIVE OR 32-bit constant	3	113	68	45	27

Status word for: **AD, OD, XOD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	0	0	–	–	–	–	–

Evaluating Conditions Using AND, OR and EXCLUSIVE OR

All logic instructions generate a result (new RLO). The first instruction in a logic string generates the new RLO from the signal state scanned. The subsequent logic instructions generate the new RL from the signal state scanned and the old RLO. The logic string ends with an instruction which limits the RLO (e.g. a memory instruction); that is, the $\overline{FC}$ bit is set to zero.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
A/AN O/ON X/XN	==0	AND/AND NOT OR/OR-NOT EXCLUSIVE OR/ EXCLUSIVE-OR-NOT Result=0 (A1=0 and A0=0)	1	75	45	30	18
	>0	Result>0 (CC1=1 and CC0=0)	1	75	45	30	18
	<0	Result<0 (CC1=0 and CC0=1)	1	75	45	30	18
	<>0	Result≠0 ((CC1=0 and CC0=1) or (CC1=1 and CC0=0))	1	75	45	30	18

Status word for: **A/AN/O/ON/X/XN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	Yes	Yes	–	–	Yes	–	Yes	Yes
Instruction affects:	–	–	–	–	–	Yes	Yes	Yes	1

Evaluating Conditions Using AND, OR and EXCLUSIVE OR, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
A/AN O/ON X/XN	>=0	Result>=0 ((CC1=1 and CC0=0) or (CC1=0 and CC0=0))	1	75	45	30	18
	<=0	Result<=0 ((CC1=0 and CC0=1) or (CC1=0 and CC0=0))	1	75	45	30	18

Status word for: **A/AN/O/ON/X/XN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	Yes	Yes	–	–	Yes	–	Yes	Yes
Instruction affects:	–	–	–	–	–	Yes	Yes	Yes	1

Evaluating Conditions Using AND, OR and EXCLUSIVE OR, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
A/AN O/ON X/XN	UO	AND/AND-NOT OR/OR-NOT EXCLUSIVE-OR/ EXCLUSIVE-OR-NOT Unordered math instruction (CC1=1 and CC0=1)	1	75	45	30	18
	OS	AND OS=1	1	75	45	30	18
	BR	AND BR=1	1	75	45	30	18
	OV	AND OV=1	1	75	45	30	18

Status word for: **A/AN/O/ON/X/XN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	Yes	Yes	Yes	Yes	Yes	Yes	–	Yes	Yes
Instruction affects:	–	–	–	–	–	Yes	Yes	Yes	1

Edge-Triggered Instructions

The current RLO is compared with the status of the instruction or “edge bit memory”. FP detects a change from “0” to “1”; FN detects a change from “1” to “0”.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
FP/FN	I/Q a.b	The positive/negative edge is indicated by RLO = 1. The bit addressed in the instruction is the auxiliary edge bit memory.	2	75	45	30	18
	M a.b		2	75	45	30	18
	L a.b1)		2	75	45	30	18
	DBX a.b		2	200	120	80	48
	DIX a.b		2	200	120	80	48
	c [d]		2	75+/200+	45+/120+	30+/80+	18+/48+
	c [AR1,m] 2)		2	75+/200+	45+/120+	30+/80+	18+/48+
	c [AR2,m] 2)		2	75+/200+	45+/120+	30+/80+	18+/48+
	[AR1,m] 2)		2	75+/200+	45+/120+	30+/80+	18+/48+
	[AR2,m] 2)		2	75+/200+	45+/120+	30+/80+	18+/48+
	Parameter 2)		2	75+/200+	45+/120+	30+/80+	18+/48+

Status word for: **FP, FN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	Yes	Yes	1

\+ Plus time required for loading the address of the instruction (see page 20)
1) Unnecessary if the bit being monitored is in the process image (local data of a block are only valid while the block is running).
2) I, Q, M, L /DB, DI

Setting/Resetting Bit Addresses

Assigning the value “1” or “0” to the addressed instruction when RLO = 1. The instructions can be dependent on the MCR (see page 96).

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
S		Set addressed bit to “1”					
R		Set addressed bit to “0”					
	I/Q a.b	Input/output	1[1]/2	75	45	30	18
	M a.b	Bit memory	1[2]/2	75	45	30	18
	L a.b	Local data bit	2	75	45	30	18
	DBX a.b	Data bit	2	200	120	80	48
	DIX a.b	Instance data bit	2	200	120	80	48
	c [d]	Memory-indirect, area-internal [3]	2	75+/200+	45+/120+	30+/80+	18+/48+
	c [AR1,m]	Register-indirect, area-internal (AR1) [3]	2	75+/200+	45+/120+	30+/80+	18+/48+
	c [AR2,m]	Register-indirect, area-internal (AR2) [3]	2	75+/200+	45+/120+	30+/80+	18+/48+
	[AR1,m]	Area-crossing (AR1) [3]	2	75+/200+	45+/120+	30+/80+	18+/48+
	[AR2,m]	Area-crossing (AR2) [3]	2	75+/200+	45+/120+	30+/80+	18+/48+
	Parameter	Via parameter	2	75+/200+	45+/120+	30+/80+	18+/48+

Status word for: **S, R**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	Yes	–	0

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing; Address area 0 to 127
2) With direct instruction addressing; Address area 0 to 255
3) I, Q, M, L / DB, DI

Setting/Resetting Bit Addresses, continued

The RLO is written to the address of the instruction. The instructions can be dependent on the MCR (see page 96).

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
=		Assign RLO					
	I/Q a.b	To input/output	1[1)]/2	75	45	30	18
	M a.b	To bit memory	1[2)]/2	75	45	30	18
	L a.b	To local data bit	2	75	45	30	18
	DBX a.b	To data bit	2	200	120	80	48
	DIX a.b	To instance data bit	2	200	120	80	48
	c [d]	Memory-indirect, area-internal [3)]	2	75+/200+	45+/120+	30+/80+	18+/48+
	c [AR1,m]	Register-indirect, area-internal (AR1) [3)]	2	75+/200+	45+/120+	30+/80+	18+/48+
	c [AR2,m]	Register-indirect, area-internal (AR2) [3)]	2	75+/200+	45+/120+	30+/80+	18+/48+
	[AR1,m]	Area-crossing (AR1) [3)]	2	75+/200+	45+/120+	30+/80+	18+/48+
	[AR2,m]	Area-crossing (AR2) [3)]	2	75+/200+	45+/120+	30+/80+	18+/48+
	Parameter	Via parameter [3)]	2	75+/200+	45+/120+	30+/80+	18+/48+

Status word for: =	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	Yes	–	0

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing; Address area 0 to 127
2) With direct instruction addressing; Address area 0 to 255
3)I, Q, M, L / DB, DI

Instructions Directly Affecting the RLO

The following instructions have a direct effect on the RLO.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
CLR		Set RLO to “0”	1	75	45	30	18

Status word for: **CLR**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	0	0	0	0

SET		Set RLO to “1”	1	75	45	30	18

Status word for: **SET**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	0	1	1	0

NOT		Negate RLO	1	75	45	30	18

Status word for: **NOT**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	Yes	–	Yes	–
Instruction affects:	–	–	–	–	–	–	1	Yes	–

SAVE		Save RLO to the BR bit	1	75	45	30	18

Status word for: **SAVE**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	Yes	–	–	–	–	–	–	–	–

Timer Instructions

Starting or resetting a timer. The time value must be in ACCU1-L. The instructions are triggered by an edge transition in the RLO; that is, when the status of the RLO has changed between two calls.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
SP	T f T [e]	Start timer as pulse on edge change from “0” to “1”	1[1)]/2	150 150+	90 90+	60 60+	36 36+
	Timer para.		2	150+	90+	60+	36+
SE	T f T [e]	Start timer as extended pulse on edge change from “0” to “1”	1[1)]/2	150 150+	90 90+	60 60+	36 36+
	Timer para.		2	150+	90+	60+	36+
SD	T f T [e]	Start timer as ON delay on edge change from “0” to “1”	1[1)]/2	150 150+	90 90+	60 60+	36 36+
	Timer para.		2	150+	90+	60+	36+

Status word for **SP, SE, SD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	–	–	0

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing Timer No.: 0 to 255

Timer Instructions, continued

In-struc-tion	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
SS	T f T [e]	Start timer as retentive ON delay on edge change from “0” to “1”	1[1)]/2	150 150+	90 90+	60 60+	36 36+
	Timer para.		2	150+	90+	60+	36+
SF	T f T [e]	Start timer as OFF delay on edge change from “0” to “1”	1[1)]/2	150 150+	90 90+	60 60+	36 36+
	Timer para.		2	150+	90+	60+	36+

Status word for **SS, SF**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	–	–	0

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing Timer No.: 0 to 255

Timer Instructions, continued

In-struc-tion	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
FR	T f T [e]	Enable timer for restarting on edge change from “0” to “1” (reset edge bit memory for starting timer)	1[1)]/2	150 150+	90 90+	60 60+	36 36+
	Timer para.		2	150+	90+	60+	36+
R	T f T [e]	Reset timer	1[1)]/2	150 150+	90 90+	60 60+	36 36+
	Timer para.		2	150+	90+	60+	36+

Status word for: **FR, R**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	–	–	0

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing Timer No.: 0 to 255

Counter Instructions

The count value must be in ACCU1-L in the form of a BCD number (0 - 999).

In-struc-tion	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
S	C f C [e]	Presetting of counter on edge change from “0” to “1”	1[1)]/2	150 150+	90 90+	60 60+	36 36+
	Counter para.		2	150+	90+	60+	36+
R	C f C [e]	Reset counter to “0” when RLO = “1”	1[1)]/2	150 150+	90 90+	60 60+	36 36+
	Counter para.		2	150+	90+	60+	36+
CU	C f C [e]	Increment counter by 1 on edge change from “0” to “1”	1[1)]/2	150 150+	90 90+	60 60+	36 36+
	Counter para.		2	150+	90+	60+	36+

Status word for: **S, R, CU**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	–	–	0

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing Counter No.: 0 to 255

Counter Instructions, continued

In-struc-tion	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
CD	C f C [e]	Decrement counter by 1 on edge change from “0” to “1”	1[1)]/2	150 150+	90 90+	60 60+	36 36+
	Counter para.		2	150+	90+	60+	36+
FR	C f C [e]	Enable counter on edge change from “0” to “1” (reset edge bit memory for up and down counting and setting the counter)	1[1)]/2	150 150+	90 90+	60 60+	36 36+
	Counter para.		2	150+	90+	60+	36+

Status word for: **CD, FR**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	–	–	0

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing Counter No.: 0 to 255

Load Instructions

Loading address identifiers into ACCU1. The contents of ACCU1 are first saved to ACCU2. The status word is not affected.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
L		Load ...					
	IB a	Input byte	1[1]/2	75	45	30	18
	QB a	Output byte	1[1]/2	75	45	30	18
	PIB a	Peripheral input byte [2]	2	75	45	30	18
	MB a	Bit memory byte	1[3]/2	75	45	30	18
	LB a	Local data byte	2	75	45	30	18
	DBB a	Data byte	2	100	60	40	24
	DIB a	Instance data byte	2	100	60	40	24
		... into ACCU1					
	g [d]	Memory-indirect, area-internal [4]	2	75+/100+	45+/60+	30+/40+	18+/24+
	g [AR1,m]	Register-indirect, area-internal (AR1) [4]	2	75+/100+	45+/60+	30+/40+	18+/24+
	g [AR2,m]	Register-indirect, area-internal (AR2) [4]	2	75+/100+	45+/60+	30+/40+	18+/24+
	B[AR1,m]	Area-crossing (AR1) [4]	2	75+/100+	45+/60+	30+/40+	18+/24+
	B[AR2,m]	Area-crossing (AR2) [4]	2	75+/100+	45+/60+	30+/40+	18+/24+
	Parameter	Via parameter [4]	2	75+/100+	45+/60+	30+/40+	18+/24+

\+ Plus time required for loading the address of the instruction (see page 20)
1) With indirect instruction addressing; Address area 0 to 127
2) Plus reaction time of the I/O module (> 1 µs)
3) With direct instruction addressing; Address area 0 to 255
4) I, Q, P, M, L / DB, DI

Load Instructions, continued

If there is a remainder of 3 following an integral division of the used addresses by 4, the execution times for instructions specified on this page are doubled.

In-struc-tion	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
L		Load ...					
	IW a	Input word	1[1)]/2	75	45	30	18
	QW	Output word	1[1)]/2	75	45	30	18
	PIW a	Peripheral input word [2)]	1[1)]/2	75	45	30	18
	MW a	Bit memory word	1[3)]/2	75	45	30	18
	LW a	Local data word	2	75	45	30	18
	DBW a	Data word	2	100	60	40	24
	DIW a	Instance data word	2	100	60	40	24
		... into ACCU1-L					
	h [d]	Memory-indirect, area-internal[4)]	2	75+/100+	45+/60+	30+/40+	18+/24+
	h [AR1,m]	Register-indirect, area-internal (AR1) [4)]	2	75+/100+	45+/60+	30+/40+	18+/24+
	h [AR2,m]	Register-indirect, area-internal (AR2) [4)]	2	75+/100+	45+/60+	30+/40+	18+/24+
	W[AR1,m]	Area-crossing (AR1) [4)]	2	75+/100+	45+/60+	30+/40+	18+/24+
	W[AR2,m]	Area-crossing (AR2) [4)]	2	75+/100+	45+/60+	30+/40+	18+/24+
	Parameter	Via parameter [4)]	2	75+/100+	45+/60+	30+/40+	18+/24+

\+ Plus time required for loading the address of the instruction (see page 20)
1) With indirect instruction addressing; Address area 0 to 127
2) Plus reaction time of the I/O module (> 1 µs)
3) With direct instruction addressing; Address area 0 to 255
4) I, Q, P, M, L / DB, DI

Load Instructions, continued

If the used address is divisible by 4without a remainder, the execution times for instructions specified on this page is doubled.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
L		Load ...					
	IDa	Input double word	1[1]/2	75	45	30	18
	QD a	Output double word	1[1]/2	75	45	30	18
	PID a	Peripheral input double word [2]	1[1]/2	75	45	30	18
	MD a	Bit memory double word	1[3]/2	75	45	30	18
	LD a	Local data double word	2	75	45	30	18
	DBD a	Data double word	2	100	60	40	24
	DID a	Instance data double word	2	100	60	40	24
		... in ACCU1					
	i [d]	Memory-indirect, area internal [4]	2	75+/100+	45+/60+	30+/40+	18+/24+
	i [AR1,m]	Register-ind., area internal (AR1) [4]	2	75+/100+	45+/60+	30+/40+	18+/24+
	i [AR2,m]	Register-ind., area internal (AR2) [4]	2	75+/100+	45+/60+	30+/40+	18+/24+
	D[AR1,m]	Area-crossing (AR1) [4]	2	75+/100+	45+/60+	30+/40+	18+/24+
	D[AR2,m]	Area-crossing (AR2) [4]	2	75+/100+	45+/60+	30+/40+	18+/24+
	Parameter	Via parameter [4]	2	75+/100+	45+/60+	30+/40+	18+/24+

\+ Plus time required for loading the address of the instruction (see page 20)
1) With indirect instruction addressing; Address area 0 to 127
2) Plus the reaction time of the I/O module (> 1 µs)
3) With direct instruction addressing; Address area 0 to 255
4) I, Q, P, M, L / DB, DI

Load Instructions, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
L		Load ...					
	k8	8-bit constant into ACCU1-LL	2	75	45	30	18
	k16	16-bit constant into ACCU1-L	2	75	45	30	18
	k32	32-bit constant into ACCU1	3	113	68	45	27
	Parameter	Load constant into ACCU1 (addressed via parameter)	2	100+	60+	40+	24+
L	2#n	Load 16-bit binary constant into ACCU1-L	2	75	45	30	18
		Load 32-bit binary constant into ACCU1	3	113	68	45	27
	B#16#p	Load 8-bit-hexadecimal constant into ACCU1-L	1	75	45	30	18
L	W#16#p	Load 16-bit hexadecimal constant into ACCU1-L	2	75	45	30	18
	DW#16#p	Load 32-bit hexadecimal constant into ACCU1	3	113	68	45	27

Load Instructions, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
L	'x'	Load 1 character	2	75	45	30	18
	'xx'	Load 2 characters	2	75	45	30	18
	'xxx'	Load 3 characters	3	113	68	45	27
	'xxxx'	Load 4 characters	3	113	68	45	27
L	D# time value	Load IEC date	3	113	68	45	27
L	S5T# time value	Load S7 time constant (16 bits)	2	75	45	30	18
L	TOD# time value	Load IEC time constant	3	113	68	45	27
L	T# time value	Load 16-bit time constant	2	75	45	30	18
		Load 32-bit time constant	3	113	68	45	27
L	C# count value	Load counter constant (BCD code)	2	75	45	30	18
L	B# (b1, b2)	Load constant as byte (b1, b2)	2	75	45	30	18
	B# (b1, b2, b3, b4)	Load constant as 4 bytes (b1, b2, b3, b4)	3	113	68	45	27

Load Instructions, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
L	P# bit pointer	Load bit pointer	3	113	68	45	27
L	L# integer	Load 32-bit integer constant	3	113	68	45	27
L	Real number	Load floating-point number	3	113	68	45	27

Load Instructions for Timers and Counters

Loading a time value or count value into ACCU1. The contents of ACCU1 are first saved to ACCU2. The bits of the status word are not affected.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
L	T f T (e)	Load time value	1[1)]/2 2	75 75+	45 45+	30 30+	18 18+
	Timer para.	Load time value (addressed via parameter)	2	75+	45+	30+	18+
L	C f C (e)	Load count value	1[1)]/2 2	75 75+	45 45+	30 30+	18 18+
	Counter para.	Load count value (addressed via parameter)	2	75+	45+	30+	18+
LC	T f T (e)	Load time value in BCD	1[1)]/2 2	75 75+	45 45+	30 30+	18 18+
	Timer para.	Load time value in BCD (addressed via parameter)	2	75+	45+	30+	18+
LC	C f C (e)	Load count value in BCD	1[1)]/2 2	75 75+	45 45+	30 30+	18 18+
	Counter para.	Load count value in BCD (addressed via parameter)	2	75+	45+	30+	18+

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing; Timer/counter No.: 0 to 255

Transfer Instructions

Transferring the contents of ACCU1 to the addressed operand. Note that some instructions are affected by the MCR (see page 96). The status word is not affected.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
T		Transfer contents of ACCU1-LL to ...					
	IB a	input byte	1[1)]/2	75	45	30	18
	QB a	output byte	1[1)]/2	75	45	30	18
	PQB a	peripheral output byte[2)]	2	75	45	30	18
	MB a	bit memory byte	1[3)]/2	75	45	30	18
	LB a	local data byte	2	75	45	30	18
	DBB a	data byte	2	100	60	40	24
	DIB a	instance data byte	2	100	60	40	24
	g [d]	Memory-indirect, area internal [4)]	2	75+/100+	45+/60+	30+/40+	18+/24+
	g [AR1,m]	Register-ind., area int. (AR1) [4)]	2	75+/100+	45+/60+	30+/40+	18+/24+
	g [AR2,m]	Register-ind., area int. (AR2) [4)]	2	75+/100+	45+/60+	30+/40+	18+/24+
	B[AR1,m]	Area-crossing (AR1) [4)]	2	75+/100+	45+/60+	30+/40+	18+/24+
	B[AR2,m]	Area-crossing (AR2) [4)]	2	75+/100+	45+/60+	30+/40+	18+/24+
	Parameter	Via parameter [4)]	2	75+/100+	45+/60+	30+/40+	18+/24+

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing; Address area 0 to 127
2) I/O acknowledgement time has to be taken into account
3) With direct instruction addressing; Address area 0 to 255
4) I, Q, P, M, L / DB, DI

Transfer Instructions, continued

If there is a remainder of 3 following an integral division of the used addresses by 4, the execution times for instructions specified on this page are doubled.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
T		Transfer contents of ACCU1-L to ...					
		input word					
	IW a	output word	1[1)]/2	75	45	30	18
	QW a	peripheral output word[2)]	1[1)]/2	75	45	30	18
	PQW a		1[1)]/2	75	45	30	18
	MW a	bit memory word	1[3)]/2	75	45	30	18
	LW a	local data word	2	75	45	30	18
	DBW a	data word	2	100	60	40	24
	DIW a	instance data word	2	100	60	40	24
	h [d]	Memory-indirect, area internal [4)]	2	75+/100+	45+/60+	30+/40+	18+/24+
	h [AR1,m]	Register-ind., area internal (AR1) [4)]	2	75+/100+	45+/60+	30+/40+	18+/24+
	h [AR2,m]	Register-ind., area internal (AR2) [4)]	2	75+/100+	45+/60+	30+/40+	18+/24+
	W[AR1,m]	Area-crossing (AR1) [4)]	2	75+/100+	45+/60+	30+/40+	18+/24+
	W[AR2,m]	Area-crossing (AR2) [4)]	2	75+/100+	45+/60+	30+/40+	18+/24+
	Parameter	Via parameter [4)]	2	75+/100+	45+/60+	30+/40+	18+/24+

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing; Address area 0 to 127
2) I/O acknowledgement time has to be taken into account
3) With direct instruction addressing; Address area 0 to 255
4) I, Q, P, M, L / DB, DI

Transfer Instructions, continued

If the used address is divisible by 4without a remainder, the execution times for instructions specified on this page is doubled.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
T		Transfer contents of ACCU1 to ...					
	ED a	Input double word	1[1]/2	75	45	30	18
	AD a	Output double word	1[1]/2	75	45	30	18
	PAD a	periph. output double word [2]	2	75	45	30	18
	MD a	Bit memory double word	1[3]/2	75	45	30	18
	LD a	Local data double word	2	75	45	30	18
	DBD a	Data double word	2	100	60	40	24
	DID a	Instance data double word	2	100	60	40	24
T	i [d]	Memory-indirect, area internal [4]	2	75+/100+	45+/60+	30+/40+	18+/24+
	i [AR1,m]	Register-ind., area int. (AR1) [4]	2	75+/100+	45+/60+	30+/40+	18+/24+
	i [AR2,m]	Register-ind., area int. (AR2) [4]	2	75+/100+	45+/60+	30+/40+	18+/24+
	D[AR1,m]	Area-crossing (AR1) [4]	2	75+/100+	45+/60+	30+/40+	18+/24+
	D[AR2,m]	Area-crossing (AR2) [4]	2	75+/100+	45+/60+	30+/40+	18+/24+
	Parameter	Via parameter [4]	2	75+/100+	45+/60+	30+/40+	18+/24+

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing; Address area 0 to 127
2) I/O acknowledgement time has to be taken into account
3) With direct instruction addressing; Address area 0 to 255
4) I, Q, P, M, L / DB, DI

Load and Transfer Instructions for Address Registers

Loading a double word from a memory area or register into address register 1 (AR1) or address register 2 (AR2). The status word is not affected.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
LAR1		Load contents from ...					
	–	ACCU1	1	150	90	60	36
	AR2	Address register 2	1	150	90	60	36
	DBD a	Data double word	2	175	105	70	45
	DID a	Instance data double word	2	175	105	70	45
	m	32-bit constant as pointer	3	150	90	60	36
	LD a	Local data double word	2	150	90	60	36
	MD a	Bit memory double word	2	150	90	60	36
		... into AR1					
LAR2		Load contents from ...					
	–	ACCU1	1	150	90	60	36
	DBD a	Data double word	2	175	105	70	45
	DID a	Instance data double word	2	175	105	70	45
	m	32-bit constant as pointer	3	150	90	60	36
	LD a	Local data double word	2	150	90	60	36
	MD a	Bit memory double word	2	150	90	60	36
		... into AR2					

Load and Transfer Instructions forAddress Registers, continued

Transferring a double word from address register 1 (AR1) or address register 2 (AR2) to a memory area or register. The contents of ACCU1 are first saved to ACCU2. The status word is not affected.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
TAR1		Transfer contents from AR1 in ...					
	–	ACCU1	1	75	45	30	18
	AR2	Address register 2	1	150	90	60	36
	DBD a	Data double word	2	100	60	40	24
	DID a	Instance data double word	2	100	60	40	24
	LD a	Local data double word	2	75	45	30	18
	MD a	Bit memory double word	2	75	45	30	18
TAR2		Transfer contents from AR2 in ...					
	–	ACCU1	1	75	45	30	18
	DBD a	Data double word	2	100	60	40	24
	DID a	Instance data double word	2	100	60	40	24
	LD a	Local data double word	2	75	45	30	18
	MD a	Bit memory double word	2	75	45	30	18
CAR		Exchange the contents of AR1 and AR2	1	150	90	60	36

Load and Transfer Instructions for the Status Word

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
L	STW	Load status word into ACCU1		75	45	30	18

Status word for: **L STW**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Instruction affects:	–	–	–	–	–	–	–	–	–

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
T	STW	Transfer ACCU1 (bits 0 to 8) to the status word		75	45	30	18

Status word for: **T STW**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Load Instructions for DB Number and DB Length

Loading the number/length of a data block into ACCU1. The old contents of ACCU1 are saved to ACCU2. The status word is not affected.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
L	DBNO	Load number of data block	1	75	45	30	18
L	DINO	Load number of instance data block	1	75	45	30	18
L	DBLG	Load length of data block into byte	1	75	45	30	18
L	DILG	Load length of instance data block into byte	1	75	45	30	18

Integer Math (16 Bits)

Math instructions on two 16-bit words. The result is written to ACCU1 and/or ACCU1-L. ACCU3 and ACCU4 are then transferred to ACCU2 and ACCU3.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
+I		Add 2 integers (16 bits) (ACCU1-L)=(ACCU1-L)+(ACCU2-L)	1	75	45	30	18
–I		Subtract 1 integer from another (16 bits) (ACCU1-L)=(ACCU2-L)-(ACCU1-L)	1	75	45	30	18

Status word for: **+I, –I,**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	–	–	–	–

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
*I		Multiply 1 integer by another (16 bits) (ACCU1)=(ACCU2-L)*(ACCU1-L)	1	75	45	30	18
/I		Divide 1 integer by another (16 bits) (ACCU1-L)=(ACCU2-L):(ACCU1-L) The remainder is in ACCU1-H	1	300	180	120	72

Status word for: ***I, /I**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	–	–	–	–

Integer Math (32 Bits)

Math instructions on two 32-bit words. The result is written to ACCU1. ACCU3 and ACCU4 are then transferred to ACCU2 and ACCU3.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
+D		Add 2 integers (32-bit) (ACCU1)=(ACCU2)+(ACCU1)	1	75	45	30	18
–D		Subtract 2 integer from another (32 bits) (ACCU1)=(ACCU2)-(ACCU1)	1	75	45	30	18
*D		Multiply 2 integer by another (32 bits) (ACCU1)=(ACCU2)*(ACCU1)	1	75	45	30	18

Status word for: **+D, –D, *D**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	–	–	–	–

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
/D		Divide 2 integer by another (32 bits) (ACCU1)=(ACCU2):(ACCU1)	1	450	270	180	108
MOD		Divide 2 integer by another (32 bits) and load the remainder into ACCU1: (ACCU1)=remainder of [(ACCU2):(ACCU1)]	1	450	270	180	108

Status word for: **/D, MOD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	–	–	–	–

Floating-Point Math (32 Bits)

The result of the math instruction is in ACCU1. ACCU3 and ACCU4 are then transferred to ACCU2 and ACCU3.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
+R		Add 2 real numbers (32 bits) (ACCU1)=(ACCU2)+(ACCU1)	1	150	90	60	36
–R		Subtract 1 real number from another (32 bits) (ACCU1)=(ACCU2)-(ACCU1)	1	150	90	60	36
*R		Multiply 1 real number by another (32 bits) (ACCU1)=(ACCU2)*(ACCU1)	1	150	90	60	36
/R		Divide 1 real number by another (32 bits) (ACCU1)=(ACCU2):(ACCU1)	1	450	270	180	108

Status word for: **+R, –R, *R, /R**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	–	–	–	–

Floating-Point Math (32 Bits), continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
NEGR		Negate the real number in ACCU1	1	75	45	30	18
ABS		Form the absolute value of the real number in ACCU1	1	75	45	30	18

Status word for: **NEGR, ABS**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

Square Root and Square Instructions (32 Bits)

The result of the instruction is in ACCU1. The SQRT instruction can be interrupted.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
SQRT		Calculate the square root of a real number in ACCU1	1	600	360	240	144
SQR		Form the square of the real number in ACCU1	1	150	90	60	36

Status word for: **SQRT, SQR**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	–	–	–	–

Logarithmic Function (32 Bits)

The result of the logarithmic function is in ACCU1. The instructions can be interrupted.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
LN		Form the natural logarithm of a real number in ACCU1	1	1575	945	630	378
EXP		Calculate the exponential value of a real number in ACCU1 to the base e (= 2.71828)	1	2400	1440	960	576

Status word for: **LN, EXP**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	–	–	–	–

Trigonometrical Functions (32 Bits)

The result of the instruction is in ACCU1. The instructions can be interrupted.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
SIN		Calculate the sine of a real number	1	1500	900	600	360
ASIN		Calculate the arcsine of a real number	1	4875	2925	1950	1170
COS		Calculate the cosine of a real number	1	1500	900	600	360
ACOS		Calculate the arccosine of a real number	1	4950	2970	1980	1188
TAN		Calculate the tangent of a real number	1	2400	1440	960	576
ATAN		Calculate the arctangent of a real number	1	1425	855	570	342

Status word for: **SIN, ASIN, COS, ACOS, TAN, ATAN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	–	–	–	–

Adding Constants

Adding integer constants and storing the result in ACCU1. The status word is not affected.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
+	i8	Add an 8-bit integer constant	1	75	45	30	18
+	i16	Add a 16-bit integer constant	2	75	45	30	18
+	i32	Add a 32-bit integer constant	3	113	68	45	27

Adding Using Address Registers

Adding a 16-bit integer to the contents of the address register. The value is either specified as an address in the instruction or is in ACCU1-L. The status word is not affected.

In-struc-tion	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
+AR1		Add the contents of ACCU1-L to those of AR1	1	150	90	60	36
+AR1	m (0 to 4095)	Add a pointer constant to the contents of AR1	2	150	90	60	36
+AR2		Add the contents of ACCU1-L to those of AR2	1	150	90	60	36
+AR2	m (0 to 4095)	Add pointer constant to the contents of AR2	2	150	90	60	36

Comparison Instructions (16-Bit Integers)

Comparing the 16-bit integers in ACCU1-L and ACCU2-L. RLO = 1 if the condition is satisfied.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
==I		ACCU2-L=ACCU1-L	1	75	45	30	18
<>I		ACCU2-L≠ACCU1-L	1	75	45	30	18
<I		ACCU2-L<ACCU1-L	1	75	45	30	18
<=I		ACCU2-L<=ACCU1-L	1	75	45	30	18
>I		ACCU2-L>ACCU1-L	1	75	45	30	18
>=I		ACCU2-L>=ACCU1-L	1	75	45	30	18

Status word for: **==I, <>I, <I, <=I, >I, >=I**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	0	–	0	Yes	Yes	1

Comparison Instructions (32-Bit Integers)

Comparing the 32-bit integers in ACCU1 and ACCU2. RLO = 1 if the condition is satisfied.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
==D		ACCU2=ACCU1	1	75	45	30	18
<>D		ACCU2≠ACCU1	1	75	45	30	18
<D		ACCU2<ACCU1	1	75	45	30	18
<=D		ACCU2<=ACCU1	1	75	45	30	18
>D		ACCU2>ACCU1	1	75	45	30	18
>=D		ACCU2>=ACCU1	1	75	45	30	18

Status word for: **==D,< >D, <D, <=D, >D, >=D**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	0	–	0	Yes	Yes	1

Comparison Instructions (32-Bit Real Numbers)

Comparing the 32-bit real numbers in ACCU1 and ACCU2. RLO = 1 if the condition is satisfied.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
==R		ACCU2=ACCU1	1	75	45	30	18
<>R		ACCU2≠ACCU1	1	75	45	30	18
<R		ACCU2<ACCU1	1	75	45	30	18
<=R		ACCU2<=ACCU1	1	75	45	30	18
>R		ACCU2>ACCU1	1	75	45	30	18
>=R		ACCU2>=ACCU1	1	75	45	30	18

Status word for: **==R, <>R, <R, <=R, >R, >=R**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	0	Yes	Yes	1

Shift Instructions

Shifting the contents of ACCU1 and ACCU1-L to the left or right by the specified number of places. If no address identifier is specified, the contents of ACCU2-LL are used as the number of places. The last bit shifted is loaded into condition code bit CC 1.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
SLW[1)]		Shift the contents of ACCU1-L to the left. Positions that become free are provided with zeros.	1	75	45	30	18
SLW	0 ... 15						
SLD		Shift the contents of ACCU1 to the left. Positions that become free are provided with zeros.	1	75	45	30	18
SLD	0 ... 32						
SRW[1)]		Shift the contents of ACCU1-L to the right. Positions that become free are provided with zeros.	1	75	45	30	18
SRW	0 ... 15						

Status word for: **SLW, SLD, SRW**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	0	0	–	–	–	–	–

1) No. of places shifted: 0 to 16

Shift Instructions, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
SRD		Shift the contents of ACCU1 to the right. Positions that become free are provided with zeros.	1	75	45	30	18
SRD	0 ... 32						
SSI[1)]		Shift the contents of ACCU1-L with sign to the right. Positions that become free are provided with with the sign (bit 15).	1	75	45	30	18
SSI	0 ... 15						
SSD		Shift the contents of ACCU1 with sign to the right. Positions that become free are provided with with the sign (bit 31).	1	75	45	30	18
SSD	0 ... 32						

Status word for: **SRD,SSI, SSD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	0	0	–	–	–	–	–

1) No. of places shifted: 0 to 16

Rotate Instructions

Rotate the contents of ACCU1 to the left or right by the specified number of places. If no address identifier is specified, the contents of ACCU2-LL are used as the number of places. The last bit shifted is loaded into condition code bit CC1.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
RLD		Rotate the contents of ACCU1 to the left	1	75	45	30	18
RLD	0 ... 32						
RRD		Rotate the contents of ACCU1 to the right	1	75	45	30	18
RRD	0 ... 32						

Status word for: **RLD, RRD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	0	0	–	–	–	–	–

Rotate Instructions, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
RLDA		Rotate the contents of ACCU1 one bit position to the left through condition code bit CC 1	1	75	45	30	18
RRDA		Rotate the contents of ACCU1 one bit position to the right through condition code bit CC 1	1	75	45	30	18

Status word for: **RLDA, RRDA**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	0	0	–	–	–	–	–

Accumulator Transfer Instructions, Incrementing and Decrementing

The status word is not affected.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
CAW		Reverse the order of the bytes in ACCU1-L.	1	75	45	30	18
CAD		Reverse the order of the bytes in ACCU1.	1	75	45	30	18
TAK		Swap the contents of ACCU1 and ACCU2	1	75	45	30	18
ENT		The contents of ACCU2 and ACCU3 are transferred to ACCU3 and ACCU4.	1	75	45	30	18
LEAVE		The contents of ACCU3 and ACCU4 are transferred to ACCU2 and ACCU3.	1	75	45	30	18
PUSH		The contents of ACCU1, ACCU2 and ACCU3 are transferred to ACCU2, ACCU3 and ACCU4	1	75	45	30	18
POP		The contents of ACCU2, ACCU3 and ACCU4 are transferred to ACCU1, ACCU2 and ACCU3	1	75	45	30	18

Accumulator Transfer Instructions, Incrementing and Decrementing, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
INC	k8	Increment ACCU1-LL	1	75	45	30	18
DEC	k8	Decrement ACCU1-LL	1	75	45	30	18

Program Display and Null Operation Instructions

The status word is not affected.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
BLD	k8	Program display instruction: Is treated by the CPU as a null operation instruction.	1	38	23	15	9
NOP	0 1	Null operation instruction	1	38	23	15	9

Data Type Conversion Instructions

The results of the conversion are in ACCU1.

Instruction	Addr. ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
BTI		Convert contents of ACCU1-L from BCD (0 to +/- 999) to integer (16 bits) (**B**CD **T**o **I**nt)	1	75	45	30	18
BTD		Convert contents of ACCU1 from BCD (0 to +/-9 999 999) to double integer (32 bits) (**B**CD **T**o **D**oubleint)	1	75	45	30	18
DTR		Convert contents of ACCU1 from double integer (32 bits) to real number (32 bits) (**D**oubleint **T**o **R**eal)	1	150	90	60	36
ITD		Convert contents of ACCU1 from integer (16 bits) to double integer (32 bits) (**I**nt **T**o **D**oubleint)	1	75	45	30	18

Status word for: **BTI, BTD, DTR, ITD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

Data Type Conversion Instructions, continued

Instruction	Addr. ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
ITB		Convert contents of ACCU1-L from integer (16 bits) to BCD from 0 to +/- 999 (**I**nt **T**o **B**CD)	1	75	45	30	18
DTB		Convert contents of ACCU1 from double integer (32 bits) to BCD from 0 to +/- 9 999 999 (**D**oubleint **T**o **B**CD)	1	75	45	30	18

Status word for: **ITB, DTB**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	Yes	Yes	–	–	–	–

Data Type Conversion Instructions, continued

The real number to be converted is in ACCU1.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
RND+		Convert a real number into a 32-bit integer. The number is rounded up to the next whole number.	1	75	45	30	18
RND		Convert a real number into a 32-bit integer.	1	75	45	30	18
RND-		Convert a real number into a 32-bit integer. The number is rounded down to the next whole number.	1	75	45	30	18
TRUNC		Convert a real number into a 32-bit integer. The places after the decimal point are truncated.	1	75	45	30	18

Status word for: **RND, RND-, RND+, TRUNC**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	Yes	Yes	–	–	–	–

Forming the Ones and Twos Complements

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
INVI		Form the ones complement of ACCU1-L	1	75	45	30	18
INVD		Form the ones complement of ACCU1	1	75	45	30	18

Status word for: **INVI, INVD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

NEGI		Form the twos complement of ACCU1-L (integer)	1	75	45	30	18
NEGD		Form the twos complement of ACCU1 (double integer)	1	75	45	30	18

Status word for: **NEGI, NEGD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	–	–	–	–

Block Call Instructions

The runtimes of the System Functions are specified in the chapter entitled “System Functions” as of page 105.

The information on the status word only relates to the block call itself and not to the commands called in this block.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
CALL	FB q, DB q	Unconditional call of an FB, with parameter transfer	15/17[1)]	2425 [2)]	1455 [2)]	880 [2)]	528 [2)]
CALL	SFB q, DB q	Unconditional call of an SFB, with parameter transfer	16/17[1)]	2425 [2)]	1455 2)	880 2)	528 [2)]
CALL	FC q	Unconditional call of a function, with parameter transfer	7/8[1)]	2100 [2)]	1260 [2)]	760 [2)]	456 [2)]
CALL	SFC q	Unconditional call of an SFC, with parameter transfer	8	2100 [2)]	1260 2)	760 2)	456 [2)]

Status word for: **CALL**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	0	0	1	–	0

1) The instruction length depends on the block number from (0...255 or more)
2) Plus time required for supplying parameters

Block Call Instructions, continued

In-struction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
UC	FB q FC q FB [e] FC [e] Parameter	Unconditional call of blocks, without parameter transfer Memory-indirect FB call Memory-indirect FC call FB/FC call via parameter	1 [1]/2 2 2 2	1450 1450 1450+ 1450+ 1450+	870 870 870+ 870+ 870+	490 490 490+ 490+ 490+	294 294 294+ 294+ 294+
CC	FB q FC q FB [e] FC [e] Parameter	Conditional call of blocks, without parameter transfer Memory-indirect FB call Memory-indirect FC call FB/FC call via parameter	1 [1]/2 2 2 2	1600/325 [3] 1600/325 [3] 1600+/325+ [3] 1600+/325+ [3] 1600+/325+ [3]	960/195 [3] 960/195 [3] 960+/195+ [3] 960+/195+ [3] 960+/195+ [3]	550/130 [3] 550/130 [3] 550+/130+ [3] 550+/130+ [3] 550+/130+ [3]	330/78 [3] 330/78 [3] 330+/78+ [3] 330+/78+ [3] 330+/78+ [3]

Status word for: **UC, CC [2]**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	– [2]	–
Instruction affects:	–	–	–	–	0	0	1	– [2]	0

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction (DB) addressing; Block No. 0 to 255
2) Instruction CC: Depending on RLO, sets RLO = 1
3) If call is not executed

Block Call Instructions, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns							
				CPU 412		CPU 414		CPU 416		CPU 417	
				1. open	2. - n. open [1]	1. open	2. - n. open [1]	1. open	2. - n. open [1]	1. open	2. - n. open [1]
OPN		Select a data block									
	DB q DI q	Direct data block, DB Direct instance DB	1[2]/2	300	75	180	45	120	30	72	18
	DB [e] DI [e]	Data block, indirect save Bit memory area M Local data area L Data block DB/DI	2	 450 450 475	 225 225 250	 270 270 295	 135 135 150	 180 180 190	 90 90 100	 108 108 114	 54 54 60
	Param.	Data block via parameters	2	475	250	295	150	190	100	114	60

Status word for: **OPN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

[1] if the same DB or DI is already selected
[2] Direct data block, DB no. 1 to 255

Block End Instructions

Instruction	Address ID	Description	Length in Words	Execution Time in ns CPU 412	CPU 414	CPU 416	CPU 417
BE		End block	1	1750	1050	700	420
BEU		End block unconditionally	1	1750	1050	700	420

Status word for: **BE, BEU**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	0	0	1	–	0

BEC		End block conditionally if RLO = “1”		1900 325 [1]	1140 195 [1]	760 130 [1]	456 78 [1]

Status word for: **BEC**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	Yes	0	1	1	0

[1] If jump is not executed

Exchanging Shared Data Block and Instance Data Block

Exchanging the two current data blocks. The current shared data block becomes the current instance data block, and vice versa. The status word is not affected.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
CDB		Exchange shared data block and instance data block	1	150	90	60	36

Jump Instructions

Jumping as a function of conditions.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
JU	LABEL	Jump unconditionally	2	500	300	210	126

Status word for: **JU**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

JC	LABEL	Jump if RLO = “1”	2	500/75 [1]	300/45 [1]	210/30 [1]	126/18 [1]
JCN	LABEL	Jump if RLO = “0”	2	500/75 [1]	300/45 [1]	210/30 [1]	126/18 [1]

Status word for: **JC, JCN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	1	1	0

[1] If jump is not executed

Jump Instructions, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
JCB	LABEL	Jump if RLO = “1”. Save the RLO in the BR bit	2	500/75 [1]	300/45 [1]	210/30 [1]	126/18 [1]
JNB	LABEL	Jump if RLO = “0”. Save the RLO in the BR bit	2	500/75 [1]	300/45 [1]	210/30 [1]	126/18 [1]

Status word for: **JCB, JNB**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	Yes	–	–	–	–	0	1	1	0

JBI	LABEL	Jump if BR = “1”	2	500/75 [1]	300/45 [1]	210/30 [1]	126/18 [1]
JNBI	LABEL	Jump if BR = “0”	2	500/75 [1]	300/45 [1]	210/30 [1]	126/18 [1]

Status word for: **JBI, JNBI**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	Yes	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	0	1	–	0

[1] If jump is not executed

Jump Instructions, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
JO	LABEL	Jump on stored overflow (OV = “1”)	2	500/75 [1]	300/45 [1]	210/30 [1]	126/18 [1]

Status word for: **JO**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	Yes	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

JOS	LABEL	Jump on stored overflow (OS = “1”)	2	500/75 [1]	300/45 [1]	210/30 [1]	126/18 [1]

Status word for: **JOS**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	Yes	–	–	–	–
Instruction affects:	–	–	–	–	0	–	–	–	–

[1] If jump is not executed

Jump Instructions, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
JUO	LABEL	Jump if “unordered math instruction” (CC1=1 and CC0=1)	2	500/75 [1]	300/45 [1]	210/30 [1]	126/18 [1]
JZ	LABEL	Jump if result = 0 (CC1=0 and CC0=0)	2	500/75 [1]	300/45 [1]	210/30 [1]	126/18 [1]
JP	LABEL	Jump if result > 0 (CC1=1 and CC0=0)	2	500/75 [1]	300/45 [1]	210/30 [1]	126/18 [1]
JM	LABEL	Jump if result < 0 (CC1=0 and CC0=1)	2	500/75 [1]	300/45 [1]	210/30 [1]	126/18 [1]
JN	LABEL	Jump if result ≠ 0 (CC1=1 and CC0=0) or (CC1=0 and CC0=1)	2	500/75 [1]	300/45 [1]	210/30 [1]	126/18 [1]

Status word for: **JUO, JZ, JP, JM, JN,**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	Yes	Yes	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

[1] If jump is not executed

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
JMZ	LABEL	Jump if result $\leq$ 0 (CC1=0 and CC0=1) or (CC1=0 and CC0=0)	2	500/75 [1]	300/45 [1]	210/30 [1]	126/18 [1]
JPZ	LABEL	Jump if result $\geq$ 0 (CC1=1 and CC0=0) or (CC1=0 and CC0=0)	2	500/75 [1]	300/45 [1]	210/30 [1]	126/18 [1]

Status word for: **JUO, JZ, JP, JM, JN, JMZ, JPZ**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	Yes	Yes	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

[1] If jump is not executed

Jump Instructions, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
JL	LABEL	Jump distributor This instruction is followed by a list of jump instructions. The address identifier is a jump label to subsequent instructions in this list. ACCU1-LL contains the number of the jump instruction to be executed (max. 254). The number of the first jump instruction is 0.	2	575	345	240	144
LOOP	LABEL	Decrement ACCU1-L and jump if ACCU1-L ≠ 0 (loop programming)	2	400/75 [1]	240/45 [1]	160/30 [1]	96/18 [1]

Status word for: **JL, LOOP**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

[1] If jump is not executed

Instructions for the Master Control Relay (MCR)

MCR=1 => MCR is deactivated. MCR=0 => MCR is activated.
“T” and “=” instructions write zeros to the corresponding address identifiers if RLO = “0”; “S” and ”R” instructions leave the memory contents unchanged. 8 MCR bracket levels per priority class are possible.

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
MCR(		Open an MCR zone. Save the RLO to the MCR stack.	1	75	45	30	18

Status word for: **MCR(**	CC1	BR	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	1	–	0

)MCR		Close an MCR zone. Pop an entry off the MCR stack.	1	75	45	30	18

Status word for: **)MCR**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	0	1	–	0

Instructions for the Master Control Relay (MCR), continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns			
				CPU 412	CPU 414	CPU 416	CPU 417
MCRA		Activate the MCR	1	75	45	30	18
MCRD		Deactivate the MCR	1	75	45	30	18

Status word for: **MCRA, MCRD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

Oganization Blocks (OB)

A user program for the S7-400 is made up of blocks containing the statements, parameters and data for the relevant CPU. The number of blocks you can create or which are provided by the operating system is different for each of the S7-400 CPUs. You will find a detailed description of the OBs and their use in the *STEP 7 Programming Manual*.

Organization Blocks	CPU 412	CPU 414	CPU 416	CPU 417	Start Events (Hexadecimal Values)
Free cycle					
OB 1	x	x	x	x	1101, 1102, 1103, 1104, 1105
Time-of-day interrupts					
OB 10	x	x	x	x	1111
OB 11	x	x	x	x	1112
OB 12		x	x	x	1113
OB 13		x	x	x	1114
OB 14			x	x	1115
OB 15			x	x	1116
OB 16			x	x	1117
OB 17			x	x	1118

Organization Blocks (OB), continued

Organization Blocks	CPU 412	CPU 414	CPU 416	CPU 417	Start Events (Hexadecimal Values)
Time-delay interrupts					
OB 20	x	x	x	x	1121
OB 21	x	x	x	x	1122
OB 22		x	x	x	1123
OB 23		x	x	x	1124
Timed interrupts					
OB 30			x	x	1131, 113A
OB 31			x	x	1132, 113A
OB 32	x	x	x	x	1133, 113A
OB 33		x	x	x	1134, 113A
OB 34		x	x	x	1135, 113A
OB 35	x	x	x	x	1136, 113A
OB 36			x	x	1137, 113A
OB 37			x	x	1138, 113A
OB 38			x	x	1139, 113A

Organization Blocks (OB), continued

Organization Blocks	CPU 412	CPU 414	CPU 416	CPU 417	Start Events (Hexadecimal Values)
Hardware interrupts					
OB 40	x	x	x	x	1141, 1142, 1143, 1144, 1145
OB 41	x	x	x	x	1141, 1142, 1143, 1144, 1145
OB 42		x	x	x	1141, 1142, 1143, 1144, 1145
OB 43		x	x	x	1141, 1142, 1143, 1144, 1145
OB 44			x	x	1141, 1142, 1143, 1144, 1145
OB 45			x	x	1141, 1142, 1143, 1144, 1145
OB 46			x	x	1141, 1142, 1143, 1144, 1145
OB 47			x	x	1141, 1142, 1143, 1144, 1145
Interrupt OBs for DPV1:					
OB 55	x	x	x	x	1155, 1158
OB 56	x	x	x	x	1156, 1159
OB 57	x	x	x	x	1157, 115A, 115B

Organization Blocks (OB), continued

Organization Blocks	CPU 412	CPU 414	CPU 416	CPU 417	Start Events (Hexadecimal Values)
Multicomputing interrupts					
OB 60	x	x	x	x	1161, 1162
Synchronous cycle interrupt:					
OB 61	x	x	x	x	1164
OB 62	x	x	x	x	1165
OB 63		x	x	x	1166
OB 64			x	x	1167
Asynchronous error interrupts:					
OB 80	x	x	x	x	3501, 3502, 3505, 3506, 3507, 3508, 3509, 350A
OB 81	x	x	x	x	3821, 3822, 3823, 3825, 3826, 3827, 3831, 3832, 3833, 3921, 3922, 3923, 3925, 3926, 3927, 3931, 3932, 3933
OB 82	x	x	x	x	3842, 3942
OB 83	x	x	x	x	3951, 3954, 3854, 3855, 3856, 3858, 3861, 3961, 3863, 3864, 3865, 3866, 3966, 3267, 3367, 3968
OB 84	x	x	x	x	3582, 3583, 3986, 3587
OB 85	x	x	x	x	35A1, 35A2, 35A3, 34A4, 35A4, 39B1, 39B2, 38B3, 39B3, 38B4, 39B4

Organization Blocks	CPU 412	CPU 414	CPU 416	CPU 417	Start Events (Hexadecimal Values)
OB 86	x	x	x	x	38C1, 39C1, 38C2, 39C3, 38C4, 39C4, 38C5, 39C5, 38C6, 38C7, 38C8, 39CA, 38CB, 39CB, 38CC, 39CD, 39CE
OB 87	x	x	x	x	35D2, 35D3, 35D4, 35D5, 35E1, 35E2, 35E3, 35E4, 35E5, 35E6
OB 88	x	x	x	x	3573, 3575, 3576
Background:					
OB 90	x	x	x	x	1191, 1192, 1193, 1195
Warm restart:					
OB 100	x	x	x	x	1381, 1382, 138A, 138B
Hot restart:					
OB 101	x	x	x	x	1383, 1384
Cold restart:					
OB 102	x	x	x	x	1385, 1386, 1387, 1388
Synchronous error interrupts:					
OB 121	x	x	x	x	2521, 2522, 2523, 2524, 2525, 2526, 2527, 2528, 2529, 2530, 2531, 2532, 2533, 2534, 2535, 253A, 253C, 253D, 253E, 253F
OB 122	x	x	x	x	2942, 2943

Function Blocks (FB)

The following tables list the quantities, numbers and maximum sizes of the function blocks you can create for the various S7-400 CPUs.

Function Blocks	CPU 412-1	CPU 412-2	CPU 414	CPU 416	CPU 417
Quantity	750	1500	3000	5000	8000
Permissible numbers	0 to 7999	0 to 7999	0 to 7999	0 to 7999	0 to 7999
Maximum size of a function block (code required for execution)	65534 bytes	65534 bytes	65534 bytes	65534 bytes	65534 bytes

Functions (FC) and Data Blocks (DB)

The following tables list the quantities, numbers and maximum sizes of the functions and data blocks you can create for the various S7-400 CPUs.

Functions	CPU 412-1	CPU 412-2	CPU 414	CPU 416	CPU 417
Quantity	750	1500	3000	5000	8000
Permissible numbers	0 to 7999	0 to 7999	0 to 7999	0 to 7999	0 to 7999
Maximum size of a function (code required for execution)	65534 bytes	65534 bytes	65534 bytes	65534 bytes	65534 bytes

Data Blocks	CPU 412-1	CPU 412-2	CPU 414	CPU 416	CPU 417
Quantity	1500	3000	6000	10000	16000
Permissible numbers	1 to 16000	1 to 16000	1 to 16000	1 to 16000	1 to 16000
Maximum size of a data block (number of data bytes)	65534 bytes	65534 bytes	65534 bytes	65534 bytes	65534 bytes

System Functions

The following tables show the system functions which are provided by the operating system of the S7-400 CPUs and the execution times for the various CPUs. (X: function available, execution times not yet available before printing).

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
0	SET_CLK	Set clock	99	73	48	29
1	READ_CLK	Read clock	16	11	8	5
2	SET_RTM	Set run-time meter	13	9	6	4
3	CTRL_RTM	Start and stop run-time meter	11	7	5	4
4	READ_RTM	Read run-time meter	14	9	7	4
5	GADR_LGC	Find logical address of a channel centralized I/O	19	14	10	6
		internal DP	24	18	12	8
6	RD_SINFO	Read start information of current OB	19	13	9	6
7	DP_PRAL	Trigger a process interrupt at the DP master First call	165	115	80	58
		Intermediate call	15	10	8	6
		Last call	15	10	8	6

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
9	EN_MSG	Enable block-related, symbol-related, and group status messages. First call, REQ = 1	79	58	40	25
		Last call	21	15	10	6
10	DIS_MSG	Disable block-related, symbol-related, and group status messages. First call, REQ = 1	79	59	41	25
		Last call	21	15	10	6

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
11	DPSYC_FR	Synchronize groups of DP Slaves First call, internal DP interface, REQ = 1	70	52	35	22
		Intermediate call, internal DP interface, BUSY = 1 [1)]	21+ n* 4	15+ n* 3	10+ n* 2	6+ n* 2
		Last call, internal DP interface, BUSY=0 [1)]	21+ n* 4	15+ n*3	10+ n* 2	7+ n* 2
11	DPSYC_FR	First call, external DP interface, REQ=1	45	37	31	26
		Intermediate call, external DP interface, BUSY = 1 [1)]	32+ n* 4	25+ n* 3	19+ n* 2	15+ n* 2
		Last call, external DP interface, BUSY= 0 [1)]	32+ n* 4	25+ n* 3	19+ n* 2	15+ n* 2

[1)] n = number of active jobs with the same logic address

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
12	D_ACT_DP	Deactivate and activate DP slaves via integrated DP interface, MODE = 0	41	29	20	12
12	D_ACT_DP	Deactivate and activate DP slaves via integrated DP interface, MODE = 1, 3 First call	136	98	70	45
		Intermediate call	43	31	21	12
		Last call	50	37	25	15
12	D_ACT_DP	Deactivate and activate DP slaves via integrated DP interface, MODE = 2, 4 First call	260	158	112	82
		Intermediate call	43	31	21	13
		Last call	51	37	25	15
12	D_ACT_DP	Deactivate and activate DP slaves via external DP interface, MODE = 0	43	30	21	12
12	D_ACT_DP	Deactivate and activate DP slaves via external DP interface, MODE = 1, 3 First call	136	99	69	40
		Intermediate call	43	31	21	13
		Last call	51	37	25	15

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
12	D_ACT_DP	Deactivate and activate DP slaves via external DP interface, MODE = 2, 4 First call	260	156	109	78
		Intermediate call	43	31	21	12
		Last call	51	37	25	14
12	D_ACT_DP	Deactivate and activate IO devices via integrated PNIO interface, MODE = 0 [1]	–	25	17	–
12	D_ACT_DP	Deactivate and activate IO devices via integrated PNIO interface, MODE = 1, 3 [1] First call	–	95	66	–
		Intermediate call	–	27	18	–
		Last call	–	33	22	–
12	D_ACT_DP	Deactivate and activate IO devices via integrated PNIO interface, MODE = 2, 4 [1] First call	–	300	200	–
		Intermediate call	–	27	18	–
		Last call	–	33	22	–
12	D_ACT_DP	Deactivate and activate IO devices via external PNIO interface, MODE = 0	43	29	21	13

[1] only for CPUs with integrated PNIO interface

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
12	D_ACT_DP	Deactivate and activate IO devices via external PNIO interface, MODE = 1, 3 First call	134	99	69	41
		Intermediate call	43	31	21	13
		Last call	51	37	25	17
12	D_ACT_DP	Deactivate and activate IO devices via external PNIO interface, MODE = 2, 4 First call	260	157	111	80
		Intermediate call	43	31	21	13
		Last call	51	37	25	15
13	DP_NRMDG	Read slave diagnostic data First call	112	84	58	36
		Intermediate call	45	35	23	16
		Last call (28 bytes)	63	46	32	22

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
14	DPRD_DAT [3]	Read consistent user data (n bytes) via integrated DP interface 3 bytes	33	24	17	10
		via integrated DP interface 32 bytes	34	25	18	11
		via external DP interface 3 bytes	42	32	30	21
		via external DP interface 32 bytes	142	114	109	88
15	DPWR_DAT [3]	Write consistent user data (n bytes) via integrated DP interface 3 bytes	32[1]/ 33[2]	24[1]/ 25[2]	16[1]/ 17[2]	11[1]/ 12[2]
		via integrated DP interface 32 bytes	33[1]/ 36[2]	25[1]/ 26[2]	17[1]/ 18[2]	11[1]/ 12[2]
		via external DP interface 3 bytes	38[1]/ 40[2]	30[1]/ 31[2]	27[1]/ 27[2]	18[1]/ 19[2]
		via external DP interface 32 bytes	91[1]/ 93[2]	83[1]/ 85[2]	81[1]/ 82[2]	75[1]/ 76[2]
17	ALARM_SQ	Generate acknowledgeable block-related messages. First call, SIG = 0 –> 1	141	114	95	44
		Empty call	59	46	41	23
18	ALARM_S	Generate unacknowledgeable block-related messages. First call, SIG = 0 –> 1	202	107	92	59
		Empty call	65	43	40	18

[1] without data transmission to the process image

[2] with data transmission to the process image

[3] There are no execution times currently available for the reading and writing of constant user data via integrated and external PNIO interfaces.

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
19	ALARM_SC	Acknowledgment status of the last ALARM_SQ entering state message.	44	30	19	12
20	BLKMOV	Copy variable within the work memory (n = number of bytes to be copied)	27 + n * 0.07	19 + n * 0.035	13 + n * 0.025	8 + n * 0.014
		Source = Load memory	352 + n * 1.05	291 + n * 0.96	243 + n * 0.65	218 + n * 0.9
21	FILL	Set array default variables within the work memory (n = length of target variables in bytes)	24 + n * 0.03	18 + n * 0.014	12 + n * 0.012	7 + n * 0.01
22	CREAT_DB	Create data block	60	45	25	18
		Occupy last free DB No. from a field of 100 DBs	266	192	114	82
23	DEL_DB	Delete data block	62	41	25	18
24	TEST_DB	Test data block	20	13	8	6
25	COM-PRESS	Compress user memory First call (trigger)	51	37	25	16
		Intermediate call (active)	10	7	5	3
26	UPDAT_PI	Update process image input table (run-time entry for 1 DI 32 in the central rack)	24	18	16	12
		AI 8* 13Bit	44	38	35	31

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
27	UPDAT_PO	Update process image output table (run-time entry for 1 DO 32 in the central rack)	23	18	15	12
		AO 8* 13Bit	41	35	32	28
28	SET_TINT	Set time-of-day interrupt	44	32	22	13
29	CAN_TINT	Cancel time-of-day interrupt	15	10	7	5
30	ACT_TINT	Activate time-of-day interrupt	30	21	15	9
31	QRY_TINT	Query time-of-day interrupt	8	5	4	2
32	SRT_DINT	Start time-delay interrupt	24	18	13	8
33	CAN_DINT	Cancel time-delay interrupt	16	11	8	5
34	QRY_DINT	Query time-delay interrupt	9	6	4	3
35	MP_ ALM	Trigger multicomputing interrupt	160	123	87	56
36	MSK_FLT	Mask synchronous faults	10	6	5	3
37	DMSK_FLT	Demask synchronous faults	11	8	6	4
38	READ_ERR	Read error register	11	8	5	4

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
39	DIS_IRT	Discard new events Block all events (MODE = 0)	84	63	45	27
		Block all events of a priority class (MODE = 1)	22	13	11	6
		Block one event (MODE = 2)	13	8	9	4
40	EN_IRT	Stop discarding events Enable all events (MODE = 0)	85	63	43	27
		Enable all events in a priority class (MODE = 1)	21	13	10	6
		Enable an event (MODE = 2)	12	7	9	4
41	DIS_AIRT	Delay interrupt events the first time delay is activated[1)]	96	71	50	30
		If the delay is already activated	8	5	4	3

[1)] When activating the delay for the first time, the SFC 41 runtime depends on the priority class in which the SFC 41 is called. The specified runtime refers to the call in OB 1. It decreases while the priority class number increases.

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
42	EN_AIRT	If other delays are present	10	7	5	3
		Stop delaying interrupt eventswhen canceling the last delay 1)	182	143	104	63
43	RE_TRIGR	Retrigger watchdog monitoring	184	62	40	25
44	REPL_VAL	Transfer substitute value to ACCU1	11	7	5	3
46	STP	Force CPU into STOP mode cannot be measured	--	--	--	--
47	WAIT	Delay program execution in addition to waiting time	8	6	4	3
48	SNC_RTCB	Synchronize slave clocks	9	6	5	3
49	LGC_GADR	Find slot with logical address (central and PROFIBUS DP)	22	16	11	7
50	RD_LGADR	Find all logical addresses of a block (run-time entry for 1 DI 32 in the central rack)	55	39	27	17

1) When cancelling the last delay, the SFC 42 runtime depends on the priority class in which the SFC 42 is called. The specified runtime refers to the call in OB 1. It decreases while the priority class number increases.

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
51	RDSYSST	“Module identification” partial list Display one data record (0111)	66	48	31	19
51	RDSYSST	”Module Identification” partial list Display all data records (0012)	128	92	61	37
		Display one data record (0112)	79	57	37	21
		Display header information (0F12)	56	41	26	15
51	RDSYSST	“Save” partial list Display one data record (0113)	71	52	33	20
51	RDSYSST	“System Areas” partial list Display all data records (0014)	78	55	36	21
		Display header information (0F14)	56	41	27	18
51	RDSYSST	“Block Types” partial list Display all data records (0015)	72	52	35	21
51	RDSYSST	“Status of Module LEDs” partial list Display status of all LEDs (0019)	127	106	73	48
		Display header information (0F19)	92	72	47	28
51	RDSYSST	“Component Identification” partial list Display all components (001C)	111	80	54	33
		Display one of the components (011C)	74	55	35	21

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
		Display header information (0F1C)	62	45	29	17
51	RDSYSST	“Interrupt status” partial list Display one data record (0222)	88	61	42	24
51	RDSYSST	“TPA /CPU assignment” partial list Assignment between all process image partitions and OBs (0025)	169	122	80	50
		Assignment between a process image partition and the corresponding OB (0125)	67	49	32	19
		Assignment between an OB and corresponding process image partitions (0225)	131	97	64	38
		Auslesen der Kopfinfo (0F25)	61	44	28	17
51	RDSYSST	“Status information communication” partial list Display status information of a communication unit (0132)	81 - 134	58 - 99	38 - 65	24 - 39
		Display status information of a communication unit (0232)	80	60	39	23
51	RDSYSST	“Modules LEDs” partial list Status of an LED (0174)	99	78	52	31

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
51	RDSYSST	"DP master system information" partial list All known DP master systems of the CPU (0090)	128	91	60	38
		A DP master system (0190)	69	50	33	20
		Header information (0F90)	59	43	29	17
51	RDSYSST	"Module status information" partial list Display status information of all inserted modules (n=number of DR) (0091)	403 + n * 22	302 +n * 19	204 + n * 16	124 + n * 14
		Display status information of all modules /racks with incorrect type indentification (0191)	330 + n * 70	219 + n * 60	146 + n * 40	101 + n * 35
		All faulty modules (0291)	297 + n * 99	220 + n * 22	147 + n * 18	92 + n * 16
		All unavailable modules (0391)	330 + n * 69	222 + n * 60	148 + n * 40	101 +n * 35
		All submodules of the host module (0591)	90	72	47	26

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
51	RDSYSST	Display the status information of all submodules of the host module in the specified rack (0991)	147 + n * 12	107 + n * 7	72 + n * 5	47 + n * 4
		Display the status information of a module with logical basic address				
		Central (0C91)	111	81	54	32
		Distributed to integrated DP interface (0C91) [1]	135	99	66	40
		Distributed to integrated PNIO interface (0C91)	–	88	59	–
		Distributed to external PNIO interface (0C91)				
		First call	178	131	88	53
		Intermediate call	122	93	62	36
		Last call	132	99	66	39

[1] only for CPUs with integrated PN/IO interface

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
51	RDSYSST	"Module status information" partial list of a module (distributed) with logical basic address (4C91)				
		First call	178	103	71	42
		Intermediate call	119	65	43	25
		Last call	132	72	48	28
		Central all modules in the specified rack (n=number DR) (0D91)	150 + n * 23	105 + n * 16	70 + n * 10	42 + n * 8
		Distributed all modules in the specified DP station / in the specified IO device (0D91)	133 - 150	86 - 99	58 - 71	36 - 49
		all assigned modules (0E91)	418	308	205	129
		Header information (0F91)	213	194	103	66

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
51	RDSYSST	"Rack/station status information" partial list Central Display setpoint status of rack 0 (0092)	72	53	34	21
		Distributed Display setpoint status of DP system 1 (0092)	303	221	146	90
51	RDSYSST	Display setpoint value of DP system1 (via external DP interface) (4092)				
		First call	120	88	60	37
		Intermediate call	71	52	35	20
		Last call	80	58	38	22
		Display activation status of DP master system 1 (via integrated DP interface) (0192)	316	192	153	93
		Central Display the actual status of rack 0 (0292)	72	53	35	20
		Distributed Display the actual status of DP system 1 (0292)	308	233	154	92

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
51	RDSYSST	Display the actual status of the stations of a DP master system (via external DP interface) (4292)				
		First call	119	87	62	36
		Intermediate call	72	53	35	20
		Last call	81	59	39	23
51	RDSYSST	Display the status of rack 0 battery buffer if at least one battery has failed (0392)	71	52	34	20
		Display the status of the entire battery buffer of a CPU (0492)	72	52	34	20
		Display the status of the 24 V supply of all racks of a CPU (0592)	72	52	34	20
		Central Display the diagnostic status of the expansion devices (0692)	138	102	67	40
		Distributed Display the diagnostic status of the DP system 1 stations (via integrated DP interface) (0692)	357	267	178	106

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
51	RDSYSST	Diagnostic status of the stations of a DP master system connected via an external DP interface (4692)				
		First call	124	90	60	37
		Intermediate call	73	53	35	21
		Last call	81	59	39	23
51	RDSYSST	Partial list “Rack / station status information”				
		Expected status of the central rack (0094)	93	67	44	27
		Expected status of the stations of an IO controller system to an integrated interface (0094) [1]	–	595	417	–
		Expected status of the stations of an IO controller system to an external interface (0094):				
		First call	156	113	78	45
		Intermediate call	105	78	51	30
		Last call	134	98	65	38

[1] only for CPUs with integrated PN/IO interface

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
51	RDSYSST	Activation status of a station of an IO controller system which is configured and disabled (0194)				
		To integrated interface [1]:	–	642	444	–
		To an external interface:				
		First call	150	114	75	45
		Intermediate call	106	78	71	31
		Last call	135	99	65	39
51	RDSYSST	Actual status of the central rack (0294)	93	68	44	27
		Actual status of the stations of an IO controller system to an integrated interface (0294)	–	642	444	–
		Actual status of the stations of an IO controller system to an external interface (0294):				
		First call	153	111	75	45
		Intermediate call	106	79	51	31
		Last call	135	99	65	39

[1] only for CPUs with integrated PN/IO interface

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
51	RDSYSST	Diagnostic status of the central rack (0694)	145	105	71	44
		Diagnostic status of the stations of an IO controller system to an integrated interface (0694) [1]	–	643	445	–
		Diagnostic status of the stations of an IO controller system to an external interface (0694):				
		First call	150	113	76	45
		Intermediate call	107	80	52	31
		Last call	135	101	66	39
		Maintenance status of the central rack (0794)	1168	828	554	351
		Maintenance status of the stations of an IO controller system to an integrated interface (0794) [1]	–	642	444	–
		Header information (0F94) (central and PROFINET IO)	78	58	37	22

[1] only for CPUs with integrated PN/IO interface

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
51	RDSYSST	"Advanced DP master system / PROFINET IO system information" partial list				
		Read out the extended information via a DP master system / PROFINET IO system to an integrated [1] or external interface (0195)	75	54	36	21
		Header information (0F95)	58	43	29	17
51	RDSYSST	Partial list "Module status information of all submodules to a specified module for PROFINET IO to an integrated interface (0696) [1]	–	63	40	–

[1] only for CPUs with integrated PN/IO interface

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
51	RDSYSST	Module status information of a module / submodule centrally or to a PROFIBUS DP- /PROFINET interface				
		Central (0C96)	91	66	42	26
		PROFIBUS DP via integrated interface (0C96)	107	80	53	31
		PROFINET IO via integrated interface (0C96) 1):	–	63	40	–
		PROFINET IO via external interface(0C96):				
		First call	156	118	79	47
		Intermediate call	106	77	50	30
		Last call	117	84	55	33
51	RDSYSST	“Diagnostic buffer” partial list Display all deliverable event information in the current operating mode (max. 21) (00A0)	77 - 155	55 - 114	38 - 77	27 - 45
		Display the latest entries (n = 1-23) (01A0)	71 + n * 6	52 + n * 4.4	34 + n * 3	20 + n * 1.5
		Display the header information (0FA0)	62	46	30	18

1) only for CPUs with integrated PN/IO interface

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
51	RDSYSST	"Diagnostic data DS 0" partial list Display via logical basic address (00B1) Central	186	140	100	70
		PROFIBUS DP (00B1)				
		First call	158	113	74	46
		Intermediate call, REQ = 0	93	66	43	28
		Last call	103	73	47	31
51	RDSYSST	"Diagnostic data DR 1" partial list Display via physical address (00B2) Display a 16–byte long DR 1	128	97	67	43

DR = Data record

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
51	RDSYSST	“Diagnostic data DR 1” partial list Display via logical basic address (00B3) Display a 16–byte long DR 1 central	215	154	112	76
		PROFIBUS DP (00B3)				
		First call	156	112	75	44
		Intermediate call	93	66	43	26
		Last call	112	80	52	33
51	RDSYSST	”Diagnostic Data DP Slave” partial list Display via configured diagnostic address (00B4)				
		First call	144	112	74	43
		Intermediate call, REQ = 0	90	65	43	26
		Last call (6 - 240 bytes)	136	100	67	40

DR = Data record

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
52	WR_USMSG	Write user entry in diagnostic buffer write with message	48	40	26	17
		Without message	46	36	24	16
54	RD_DPARAM	Read dynamic parameters local AI 8*13 bits	76	55	36	23
		PROFIBUS DP AI 8*12 bits (DS1 = 14 bytes)	89	65	43	27
55	WR_PARM	Write dynamic parameters local AI 8*13 bits	201	160	118	87
		PROFIBUS DP First call AI 8*12 bits (14 - 240 bytes)	150	111	75	47
		PROFIBUS DP Intermediate/last call, REQ = 0	75	54	37	23
56	WR_DPARM	Write predefined dynamic parameters AI 8*13 bits Local	241	197	155	123
		PROFIBUS DP First call AI 8*12 bits (2 - 240 bytes)	119	89	60	37
		PROFIBUS DP Intermediate/last call	64	47	32	20

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
57	PARM_MOD	Assign module parameters local Module/DS number/DS lengths in bytes AI 8*13 bits	407	337	269	214
		PROFIBUS DP AO 8*12 bits First call (16 - 240 bytes)	117	87	60	37
		PROFIBUS DP Intermediate/last call	64	46	31	19

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
58	WR_REC	Write parameter data record local (n = number of bytes)	151 + n * 3	108 + n * 2.5	75 + n * 2.3	55 + n * 2.2
		First call, integrated DP interface module (n = number of bytes)	138 + n * 0.1	98 + n * 0.04	67 + n * 0.03	42 + n * 0.02
		Intermediate call, REQ = 0 integrated DP interface module	60	42	28	18
		Last call, integrated DP interface module	62	43	29	18
		First call, external DP interface module (n = number of bytes)	135 + n * 0.06	95 + n * 0.06	65 + n * 0.04	49 + n * 0.03
		Intermediate call, REQ = 0 external DP interface module	62	43	33	21
		Last call, external DP interface module	63	44	33	21

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
59	RD_REC	Read data record local (n = number of bytes)	139 + n * 3.2	106 + n * 2.7	76 + n * 2.4	56 + n * 2.2
		First call, integrated DP interface module	126	92	63	40
		Intermediate call, REQ = 0 integrated DP interface module	60	42	28	18
		Last call, integrated DP interface module (n = number of bytes)	98 + n * 0.04	76 + n * 0.04	52 + n * 0.03	34 + n * 0.02
		First call, external DP interface module	127	90	65	42
		Intermediate call, REQ = 0 external DP interface module	60	42	30	19
		Last call, external DP interface module (n = number of bytes)	96 + n * 0.06	75 + n * 0.06	55 + n * 0.03	37 + n * 0.02
60	GD_SND	Send GD packet 1 byte	118	84	65	48
		32 bytes	325	210	162	133

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
61	GD_RCV	Receive GD package (1 - 32 Byte)	58	42	35	22
62	CONTROL	Check status of the connection belonging to a local communication-SFB-instance	60	43	35	22
64	TIME_TCK	Display millisecond timer	9	6	5	3
65	X_SEND	Transmit data to external partner First call, establish a connection (1 - 76 bytes) REQ = 1	282	244	224	144
		First call, connection present (1-76 bytes)	212	160	108	64
		Intermediate call (1-76 bytes)	80	63	42	24
		Last call, BUSY = 0	87	75	51	27
66	X_RCV	Receive data from external partner Test reception (1-76 bytes)	51	34	23	16
		Read data (1-76 bytes)	151	108	74	46

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
67	X_GET	Read data from external partner First call, establish a connection (1-76 bytes) REQ = 1	243	217	206	133
		First call, connection present (1-76 bytes)	175	132	92	53
		Intermediate call (1-76 bytes)	81	65	43	24
		Last call BUSY = 0	144	117	80	44
68	X_PUT	Write data to external partner First call, establish a connection (1-76 bytes) REQ = 1	284	252	227	146
		First call, connection present (1-76 bytes)	213	176	110	66
		Intermediate call (1-76 bytes)	82	64	43	25
		Last call, BUSY = 0	90	77	52	27

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
69	X_ABORT	Abort connection to external partner First call, REQ = 1	134	88	58	37
		Intermediate call	65	41	25	17
		Last call, BUSY = 0	223	217	208	93
70	GEO_LOG	Determine the start address from the slot of a module	28	20	13	8
71	LOG_GEO	Determine the module slot from the associated logical address	26	18	12	8
72	I_GET	Read data from internal partner First call, establish a connection (1-76 bytes) REQ = 1	271	233	218	140
		First call, connection present (1-76 bytes)	218	139	95	57
		Intermediate call (1-76 bytes)	85	67	45	25
		Last call, BUSY = 0	151	122	82	46
73	I_PUT	Write data to internal partner First call, establish a connection (1-76 bytes) REQ = 1	226 - 311	171 - 265	118 - 241	70 - 153
		First call, connection present (1-76 bytes)	220	167	113	68
		Intermediate call (1-76 bytes)	84	66	44	26
		Last call, BUSY = 0	92	80	53	28

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
74	I_ABORT	Abort connection to internal partner First call, REQ = 1	113	83	58	35
		Intermediate call	57	38	25	18
		Last call, without / with connection BUSY = 0	58 / 210	40 / 193	28 / 135	20 / 93
78	OB_RT	Determine OB program runtime	25	19	13	8
79	SET [1)]	Set bit array in I/O area n = number of bits to set at 1	18 + n * 0.15	13 + n * 0.13	10 + n * 0.1	7 + n * 0.13
80	RSET [1)]	Delete bit array in I/O area n = number of bits to set at 0	17 + n * 0.15	13 + n * 0.13	9 + n * 0.1	7 + n * 0.13
81	UBLKMOV	Copy variable without interruption n = number of bytes to copy	23 + n * 0.035	16 + n * 0.03	11 + n * 0.02	7 + n * 0.01
87	C_DIAG	Determine current connection status MODE = 0	13	9	6	4
		Mode = 1, 2, 3	89	67	55	52

[1)] Measured with I/O modules of the type “Binary Simulator C79459-A1002-A1, Release 1” in the central rack

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
100	SET_CLKS	Set time-of-day and clock status MODE = 1	99	73	48	29
		MODE = 2	50	36	24	15
		MODE = 3	96	70	47	29
101	RTM	Handle operating hours counter Mode = 0 Read	15	12	8	5
		Mode = 1, 2 Start/Sop	20	16	10	6
		Mode = 4, 5, 6 Set	27	21	13	8
103	DP_TOPOL	Detemine bus topology in a DP master system first call, REQ = 1	127	94	65	48
		Intermediate call	21	16	11	8
		Last call BUSY = 0	22	17	12	8
104	CIR	Controls the CiR procedure MODE = 0, information	9	6	5	3
		MODE = 1, Enable CiR procedure	8	5	5	3
		MODE = 2, Disable CiR procefure entirely	8	5	5	3
		MODE = 3, Disable CiR procedure partially	8	5	5	3

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
105	READ_SI	Read dynamically assigned system resources MODE = 0	63 - 1972 1)	46 - 1283 1)	31 - 3575 1)	21 - 3138 1)
		MODE = 1	79 - 2107 2)	52 - 2373 2)	35 - 4006 2)	23 - 2649 2)
		MODE = 2	80 - 1809 2)	52 - 1987 2)	36 - 3309 2)	23 - 2428 2)
		MODE = 3	84 - 2217 3)	53 - 2362 3)	36 - 4012 3)	23 - 2990 3)

1) Depending on the size of the SYS_INST target area and on the number of the system resources to be read

2) Depending on the number of active messages (assigned system resources)

3) Depending on the number of active messages (assigned system resources) and on the number of assigned instances with the desired CMP_ID.

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
106	DEL_SI	Enable dynamically assigned system resources MODE = 1	89 - 1504 [1]	61 - 1641 [1]	41 - 2672 [1]	27 - 1764 [1]
		MODE = 2	90 - 1487 [1]	62 - 1610 [1]	42 - 2617 [1]	28 - 1765 [1]
		MODE = 3	88 - 1578 [2]	60 - 1660 [2]	41 - 2697 [2]	28 - 1780 [2]
107	ALARM_DQ	Acknowledgeable block-related messages create first call, SIG = 0 -> 1	147	131	78	46
		Call (without message)	62	52	33	17
108	ALARM_D	Not acknowledgeable block-related messages create first call, SIG = 0 -> 1	141	110	75	36
		Call (without message)	62	46	31	15
109	PROTECT	Activate write protection	11	8	5	3

[1] Depending on the number of active messages (assigned system resources)

[2] Depending on the number of active messages (assigned system resources) and on the number of assigned instances with the desired CMP_ID.

SFC No.	SFC Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
112	PN_IN	Update the inputs for the user program interface of the PROFINET CBA components	–	< 9750 [1)]	< 6730 [1)]	–
113	PN_OUT	Update the outputs for the user program interface of the PROFINET CBA components	–	< 8150 [1)]	< 6050 [1)]	–
114	PN_DP	Update the DP interconnections	–	< 2030 [1)]	< 2030 [1)]	–
126	SYNC_PI	Update the process image partition of the inputs in a synchronous cycle	35	25	19	15
127	SYNC_PO	Update the process image partition of the outputs in a synchronous cycle	34	24	18	15

1) Only for the CPUs 414-3 PN/DP, 416-3 PN/DP, 416F-3 PN/DP. The execution times of these blocks depend on their interconnection configuration and the size of the interface DBs. Please also note the information in chapter “CBA Reaction times” in the manual *Automation System S7–400 CPU Specifications* .

System Function Blocks

The following table lists the system function blocks provided with the operating system of the S7-400 CPUs as well as the execution times of the individual CPUs (X: function exists, execution times were not available when manual was printed).

SFB No.	SFB Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
0	CTU	Count up	2	1	1	1
1	CTD	Count down	2	1	1	1
2	CTUD	Count up and down	2	2	1	1
3	TP	Generate pulse	10	9	5	3
4	TON	Generate on-delay	10	8	5	4
5	TOF	Generate off-delay	8	6	4	3
8	USEND	Send data without coordination (one send parameter supplied) JOB activated (1 - 440 bytes)	208 - 228	157 - 172	107 - 120	66 - 70
		JOB checked	75	57	38	23
		JOB finished (DONE = 1)	73	55	37	22

SFB No.	SFB Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
9	URCV	Receive data without coordination (one receive parameter supplied) JOB activated	63	47	32	19
		JOB checked	68	50	34	21
		JOB finished (NDR = 1; 1 - 440 bytes)	145 - 164	109 - 125	73 - 83	44 - 51
12	BSEND	Send data block by block JOB activated (1 - 3000 bytes)	182	140	96	57
		JOB checked	82	62	41	25
		JOB finished (DONE = 1)	79	61	40	24
13	BRCV	Receive data block by block JOB activated (1 - 3000 bytes)	91	66	45	28
		JOB checked	94	70	47	29
		JOB finished	78	60	40	26

SFB No.	SFB Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
14	GET	Read data from remote CPU (one area specified) JOB activated	159	117	82	51
		JOB checked	76	57	38	23
		JOB finished (NDR = 1; 1 - 450 bytes)	143 - 163	108 - 123	72 - 82	44 - 51
15	PUT	Write data to remote CPU JOB activated (1 - 404 bytes)	220 - 238	165 - 180	112 - 124	69 - 75
		JOB checked	76	57	38	23
		JOB finished (DONE = 1)	72	56	37	22
16	PRINT	Send data to a printer JOB activated, REQ = 1	226 - 246	169 - 182	116 - 127	68 - 77
		JOB checked	75	56	37	23
		JOB finished, DONE = 1	74	55	36	22

SFB No.	SFB Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
19	START	Start remote device JOB activated, REQ = 1	209	161	110	67
		JOB checked	79	61	40	24
		JOB finished, DONE = 1	77	60	40	23
20	STOP	Stop remote device JOB activated, REQ = 1	211	156	108	66
		JOB checked	80	60	40	24
		JOB finished, DONE = 1	78	59	40	23
21	RESUME	Restart remote device JOB activated, REQ = 1	215	160	111	67
		JOB checked	79	60	40	24
		JOB finished, DONE = 1	77	59	39	23
22	STATUS	Query status of remote partner JOB activated, REQ = 1	130	99	68	41
		JOB checked	76	57	38	23
		JOB finished, NDR = 1	222	167	111	67

SFB No.	SFB Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
23	USTATUS	Receive status of remote device without coordination JOB activated, NDR = 1	69	51	34	21
		JOB checked	67	51	34	21
		JOB finished	223	167	112	67
31	NOTIFY_8P	Generate block–related message without acknowledgment First call or JOB activated, SIG = 0–> 1 (1 - 420 bytes)	265 - 283	203 - 215	136 - 142	84 - 88
		JOB checked	105	80	53	32
		JOB finished, DONE = 1	107	82	54	33
32	DRUM	Implement sequencer	17	13	9	6
33	ALARM	Generate block-related message with acknowledgment First call or JOB activated, SIG = 0–> 1 (1 - 420 bytes)	265 - 282	198 - 212	135 - 147	83 - 88
		JOB checked	106	80	53	32
		JOB finished, DONE = 1	107	81	54	33

SFB No.	SFB Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
34	ALARM_8	Generate block-related message without accompanying values for 8 signals First call or JOB activated, SIG = 0–> 1 (1 - 420 bytes)	206	153	106	64
		JOB checked	106	80	53	32
		JOB finished, DONE = 1	106	80	53	32
35	ALARM_8P	Generate block-related message with accompanying values for 8 signals First call or JOB activated, SIG = 0–> 1 (1 - 420 bytes)	263 - 281	199 - 213	135 - 145	83 - 89
		JOB checked	106	80	53	32
		JOB finished, DONE = 1	106	81	54	32
36	NOTIFY	Generate block-related message without acknowledgment First call or JOB activated, SIG = 0–> 1 (1 - 420 bytes)	264 - 281	200 - 212	135 - 146	80 - 89
		JOB checked	105	78	52	32
		JOB finished, DONE = 1	107	81	54	33

SFB No.	SFB Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
37	AR_SEND	Send archive data First call or JOB activated, REQ = 1 (1 - 3000 bytes)	183	138	96	54
		JOB checked	82	62	41	25
		JOB finished, DONE = 1	80	61	41	24
52	RDREC	Read data record from a central module.	164	128	93	65
52	RDREC	Read data record from a DP slave via integrated DP interface, First call (2-16 bytes)	134	101	69	43
		Intermediate call	67	50	33	20
		Last call	113	86	59	37
52	RDREC	Read data record from a DP slave via external DP interface, First call (4-16 bytes)	135	101	68	42
		Intermediate call	66	50	33	20
		Last call	111	81	55	34

SFB No.	SFB Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
52	RDREC	Read data record from an IO device via integrated PNIO interface [1], First call	–	101	68	–
		Intermediate call	–	48	32	–
		Last call	–	82	55	–
52	RDREC	Read data record from an IO device via external PNIO interface, First call	134	98	69	41
		Intermediate call	65	50	32	20
		Last call	112	78	55	34
53	WRREC	Write data record to a central module	158	125	89	60
53	WRREC	Write data record in a DP slalve via integrated DP interface, First call (1-10 bytes)	147	110	75	46
		Intermediate call	65	49	33	20
		Last call	67	50	35	21

[1] only for CPUs with integrated PNIO interface

SFB No.	SFB Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
53	WRREC	Write data record in a DP slave via external DP interface, First call (2-14 bytes)	147	111	73	45
		Intermediate call	65	49	33	20
		Last call	68	52	34	21
53	WRREC	Write data record in an IO device via integrated PNIO interface 1), First call (1-10 bytes)	–	110	74	–
		Intermediate call	–	47	31	–
		Last call	–	50	33	–
53	WRREC	Write data record in an IO device via external PNIO interface, First call (2-14 bytes)	144	111	75	45
		Intermediate call	64	48	32	20
		Last call	68	51	33	21
54	RALRM	Receive interrupt from a DP slave or an IO device Runtime measurement for non-I/O-dependent OBs, MODE = 1, OB 1	64	49	34	20

1) only for CPUs with integrated PNIO interface

SFB No.	SFB Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
54	RALRM	Receive interrupt from a DP slave or an IO device Runtime measurement at integrated DP or PROFINET interface [1], MODE = 1, OB 40, OB 83, OB 86	124	91	65	46
		OB 55 to OB 57, OB 82	126	93	67	48
54	RALRM	Receive interrupt from a DP slave or an IO device Runtime measurement at external DP or external PROFINET interface, MODE = 1, OB 40, OB 83, OB 86	204	158	110	78
		OB 55 to OB 57, OB 82	360	278	198	135
54	RALRM	Receive interrupt from a DP slave or an IO device Runtime measurement at central I/O, MODE = 1, OB 40, OB 82, OB 83, OB 86	135	79	55	36
		OB 55 to OB 57	382	288	200	142

[1] only for CPUs with integrated PNIO interface

SFB No.	SFB Name	Function	Execution Time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
81	RD_DPAR	Read predefined parameter centrally	103	77	51	28
81	RD_DPAR	Read predefined parameter DP	112	85	57	30
81	RD_DPAR	Read predefined parameter PNIO [1]				
		First call	147	115	78	45
		Intermediate call	147	117	80	45
		Last call	104	81	54	32

[1] This is only available via an external PNIO interface for all CPUs, except for the CPU 414-3 PN/DP, 416-3 PN/DP and 416F-3 PN/DP.

Function Blocks for Open Communication via Industrial Ethernet

The following table lists the function blocks for open communication via Industrial Ethernet which are made available to the S7-400 CPU by the operating system and the execution times of the corresponding CPU. The execution times are only valid for data volumes up to 8 Kbyte.

FB-Nr.	FB-Name	Meaning	Execution time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
63	TSEND [1]	Send data CP and ISO on TCP (n bytes)				
		First call	167 + n * 0.045	125 + n * 0.035	75 + n * 0.027	45 + n * 0.025
		Intermediate call	57	43	25	15
		Last call	60	45	27	15
64	TRCV [1]	Receive data via TCP and ISO on TCP (n bytes)	105 + n * 0.04	79 + n * 0.03	49 + n * 0.03	35 + n * 0.02
65	TCON	Establish connection				
		First call	128	96	62	44
		Intermediate call	38	28	18	13
		Last call	38	28	18	13

[1] The protocol “TCP” is only supported by the CPUs 414-3 PN/DP, 416-3 PN/DP and 416F-3 PN/DP.

FB-Nr.	FB-Name	Meaning	Execution time in µs			
			CPU 412	CPU 414	CPU 416	CPU 417
66	TDISCON	Terminate connection				
		First call	84	63	41	29
		Intermediate call	34	25	16	12
		Last call	35	26	17	12
67	TUSEND [1]	Send data via UDP (n bytes)				
		First call	–	129 + n * 0.034	88 + n * 0.023	–
		Intermediate call	–	40	26	–
		Last call	–	42	28	–
68	TURCV [1]	Receive data via UDP (n bytes)	–	93 + n * 0.037	62 + n * 0.026	–

[1] only for the CPUs 414-3 PN/DP, 416-3 PN/DP and 416F-3 PN/DP

Sublist of the System Status List (SSL)

SSL-ID	Information Functions
	Module Identification
0111	One ident. data record only
	CPU Characteristics
0012	CPU features, all features
0112	Features of a group
0F12	Only SSL partial list header information
	User Memory Area
0113	Data record for specified memory area
	Work memory
	System Areas
0014	System areas, all system areas
0F14	Only partial list header information
	Block Types
0015	Block types, data records for all block types

Sublist of the System Status List (SSL), continued

SSL-ID	Information Functions
	Status Module LEDs
0019	Status of all module LEDs
0F19	Only partial list header information
	Component Identification
001C	Identification of all components
011C	Identification of one component
0F1C	Only SSL partial list header information
	Interrupt Status
0222	Data record for specified interrupt
	Assignment between process image partitions and OBs
0025	Assignment betweeen all process image partitions and OBs within the CPU
0125	Assignment between a process image partition and the corresponding OB
0225	Assignment between an OB and the corresponding process image partitions
0F25	Only SSL partial list header information

Sublist of the System Status List (SSL), continued

SSL-ID	Information Functions
	Communication Status Data
0132	Status data for a communication unit
	Diagnostic status
	Target system status
0232	Status data for a communication unit
	CPU protection level, operating switch positions and version ID / CRC
	Status of the Module LEDs
0174	Status of one LED
	DP Master System Information
0090	Information about all the DP master systems known to the CPU
0190	Information about a DP master system
0F90	Only SSL partial list header information

Sublist of the System Status List (SSL), continued

	Module Status Information (A maximum of 27 data records are supplied)
0091	Module status information of all inserted modules/submodules
0191	Status information of all modules/racks with incorrect type IDs.
0291	Module status information of all faulty modules
0391	Module status information of all unavailable modules
0591	Module status information of all submodules of the host module
0991	Status information of a DP master system
0C91	Status information of a module in the central rack or connected to an integrated DP interface module or connected to an integrated PROFINET interface module
4C91	Status information of a module connected to an external DP interface module or connected to an external PROFINET interface module
0D91	Status information of all modules in the specified rack / in the specified station (DP or PROFINET)
0E91	Status information of all assigned modules

Sublist of the System Status List (SSL), continued

SSL-ID	Information Functions
	Rack/Station Status Information
0092	Expected status of the central racks/stations of a DP master system
4092	Expected status of the stations of a DP master system which is connected via an external DP interface module
0192	Activation status of the stations of a DP master system which is connected via an external DP interface module
0292	Actual status of the central racks/stations of a DP master system
4292	Actual status of the stations of a DP master system which is connected via an external DP interface module
0392	Status of the back–up battery of a CPU rack if at least one battery fails
0492	Status of the entire back–up batteries of all racks of the a CPU
0592	Actual status of the racks in the central configuration/stations of DP master system which is connected via an external DP interface module.
0692	OK status of the expansion units in the central configuration/stations of a DP master system which is connected via an integrated DP interface module.
4692	OK status of the stations of a DP master system which is connected via an external DP interface module.

Sublist of the System Status List (SSL), continued

SSL-ID	Information Functions
	Rack / station status information
0094	Expected status of the central racks / stations of an I/O controller system which is connected via an integrated interface
0194	Activation status of a station in an I/O controller system which is configured and disabled
0294	The actual status of the central racks / stations of an I/O controller system which is connected via an integrated interface
0694	Status of the expansion devices of an I/O controller system which is connected via an integrated interface
0794	Maintenance status of the central racks / stations of an I/O controler system
0F94	Only SZL partial list header information Teilistenkopfinformation
	Addtional DP Master System / PROFINET IO System Information
0195	Additional information on a DP master system / PROFINET IO system
0F95	Only SSL partial list header information
	Module status information PROFINET IO and PROFIBUS DP
0696	Module status information for all submodules in the specified module
0C96	Module status information for a central module / submodule or a PROFIBUS DP / PROFINET IO interface

Sublist of the System Status List (SSL), continued

SSL-ID	Information Functions
	Diagnostic Buffer (A maximum of 21 data records are supplied)
00A0	All current diagnostic entries available in current operating mode
01A0	The last entries
0FA0	Only partial list header information
	Module Diagnostic Data
00B1	First four diagnostic bytes of a module (DS0)
00B2	All diagnostic data of a module ($\leq$ 220 bytes, DS1) (no DP module)
00B3	All diagnostic data of a module ($\leq$ 220 bytes, DS1)
00B4	Diagnostic data of a DP slave with logical base address

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